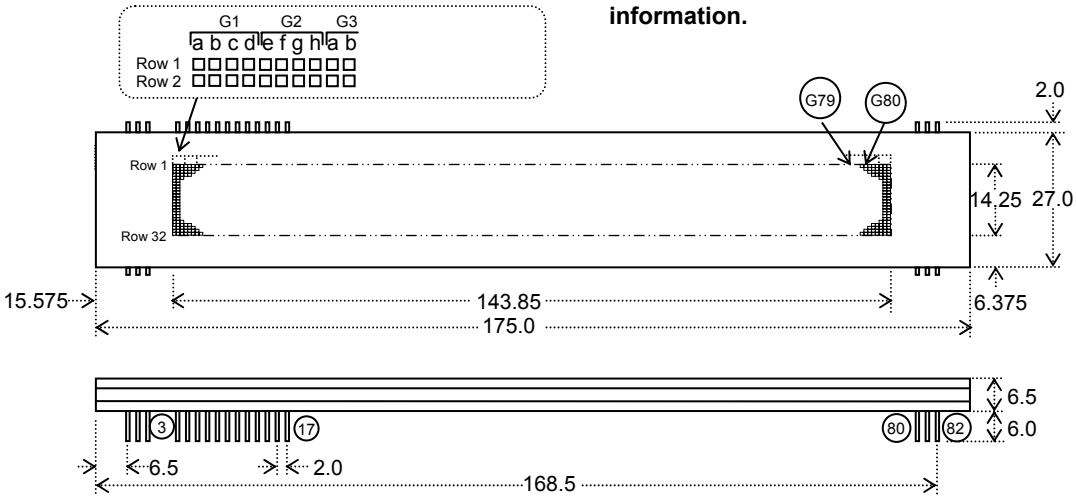
Graphic Dot Matrix Chip In Glass VFD MN32032A

- **320 x 32 Graphic Dot Matrix**
- **Chip in Glass Driver IC**
- **High Brightness Blue Green Display**
- **Synchronous Serial Interface**
- **Grey Scale Levels available**
- **Wide Operating Temperature**

This VF glass includes 2 x 336 bit serial shift register, latched drivers which connect to the anode and grid electrodes. An external host is required to provide a multiplexing data stream to refresh the display. The signal inputs can be connected to the ports of a CMOS microprocessor. The a.c. filament supply (F1, F2) can be derived from a source of 10KHz to 200KHz. Consult our application notes for further information.



Dimensions in mm. See full spec for tolerances

PIN OUT

Pin	Sig	Pin	Sig
1	F1	12	GCP
2	F1	13	SOUT2
3	F1	14	SOUT1
6	V_{DD2}	15	CLK
7	V_{SS}	16	SIN1
8	V_{SS}	17	SIN2
9	V_{DD1}	80	F2
10	BLK	81	F2
11	LAT	82	F2

ELECTRICAL SPECIFICATION

Parameter	Sym	Min	Typ	Max	Unit	Condition
Logic Voltage	V_{DD1}	3.0	3.3	5.5	V	V_{SS}=0V
Logic Current	I_{DD1}	-	2.0	4.0	mA	V_{DD1}=3.3V
Filament Voltage	E f	5.9	6.5	7.2	Vac	V_{DD2}=0V
Filament Current	I f	135	150	165	mAac	V_{DD2}=0V
Display Voltage	V_{DD2}	50.0	55.0	37.0	V	V_{SS}=0V
Display Current	I_{DD2}	-	18.0	25.0	mA	V_{DD2}=55V
Filament Bias	E_K	-	5.5	-	V	V_{SS}=0V
Logic High Input	V_{IH}	$V_{DD1x0.85}$	-	V_{DD1}	V	V_{SS}=0V
Logic Low Input	V_{IL}	0	-	x0.15	V	V_{SS}=0V
Logic High Input	I_{IH}	-	-	5.0	µA	V_{DD1}=3.3V
Logic Low Input	I_{IL}	-250	-70	-35	µA	V_{DD1}=3.3V

ENVIRONMENTAL and OPTICAL SPECIFICATION

Parameter	Value
Display Area (XxY mm)	143.85 x 14.25
Dot Size/Pitch (XxY mm)	0.3 x 0.3/0.45 x 0.45
Luminance	700 cd/m^2 typ.
Colour of Illumination	Blue-Green (Filter for colours)
Operating Temperature	-40°C to +85°C
Storage Temperature	-50°C to +85°C
Operating Humidity (non condensing)	5 to 95% @ 25°C

1. The power on rise time should be less than 50ms.
2. The 22R resistor at the V_{DD2} input is required to prevent current surge during switching.
3. If scanning of the display stops with V_{DD2} applied, the BLK input must be set high to prevent damage to the display.

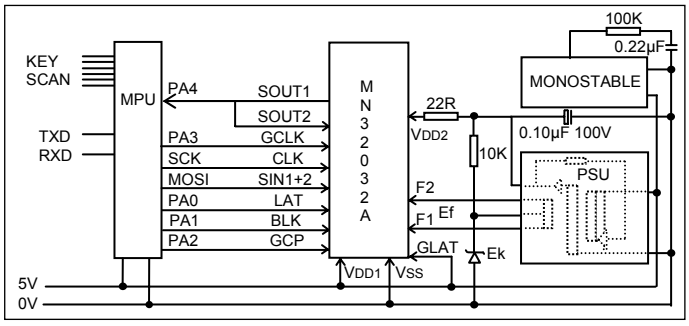
SHIFT REGISTER ASSIGNMENT

Electrode	Bit Numbers
Grid G80-G1	GSIN 257-336
Row 1 'ahbgcfde'	SIN 1-8
Row 2 'ahbgcfde'	SIN 9-16
Row 3 'ahbgcfde'	SIN 17-24
:	:
:	:
Row 31 'ahbgcfde'	SIN 241-248
Row 32 'ahbgcfde'	SIN 249-256

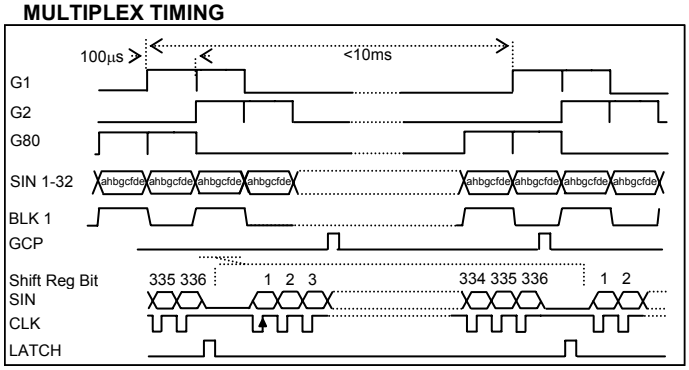
INTERFACE TIMING

Parameter	Time
CLK Cycle	300ns min
CLK High	140ns min
CLK Low	140ns min
SIN Setup	60ns min
SIN Hold	60ns min
LAT High	250ns min
CLK then LAT	200ns min
BLK Hold	5µs min

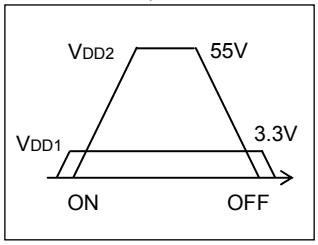
INTERFACE EXAMPLE



MULTIPLEX TIMING



POWER SEQUENCE



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Doc Ref: 04824 Iss.2 5July06