MTK-20141

"DynaMiTe™" PCI
ADSL Modem Chipset

Product Brief
Rev. 0.1 – May 1999

Applications

- **ADSL PC NICs**
- **Other ADSL systems with PCI interface**

Features

- **Support for multiple ADSL standards:**
  - **ANSI T1.413 Issue2**
  - **ITU G.992.1 (G.dmt)**
  - **ITU G.992.2 (G.lite)**
- **Integrated PCI interface**
  - **Two-chip PCI chipset solution (plus line driver)**
  - **Direct interface to 3 V/5 V PCI**
  - **PCI V2.2 compliant (with power management)**
- **Maximum downstream rate of 8 Mbps**
- **Maximum upstream rate of 832 kbps**
- **Programmable architecture facilitates quick and easy modem software upgrades**
- **Exceeds all G.lite reach requirements**
- **G.lite support for distributed filter/splitterless operation**
- **Host software targetted for Win98/NT4/Win2K* implementation with installation software, miniport drivers, and control panel software**
- **Support for PPP over ATM, native ATM and RFC1483 encapsulations**
- **Complete modem package**
  - **No dependency on external processor**
  - **Easy to use command interface**
  - **Full reference design kit for manufacture**
- **Low power, High performance**

(*) Win98/NT4/Win2K are trademarks of Microsoft Co

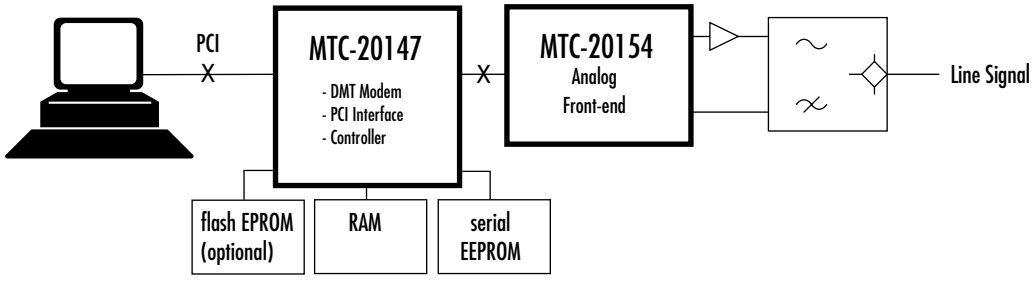

Fig.1: General Block Diagram

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General Description

The MTK-20141 is a 5th generation PCI ADSL DynaMiTe chipset from Alcatel Microelectronics. It provides all the required functions to implement a complete PCI-based, rate adaptive DMT ADSL modem. It consists of an optimised Analog Front-End (MTC-20154) and a DMT modem with embedded controller, ATM framer, and integrated PCI interface (MTC-20147).

The chipset interfaces have been defined to allow direct integration into PCI designs, reducing both time-to-market and implementation risks. ATM cells are transferred over the PCI interface.

The chipset employs Discrete Multi-tone modulation as specified in ANSI T1.413. It also complies with ITU G-dmt and G-Lite. Additional Reed Solomon forward error correction with or without interleaving provides maximum noise immunity.

The Modem Environment

An external ADSL-compatible line driver is used to drive the telephone twisted pair, and an analog POTS splitter is needed to split the baseband analog telephone signal from the modulated ADSL signal. In G-Lite mode, the splitter can be removed and replaced by distributed POTS filters. Brief characteristics of the system are given in Table 1. Table 2 shows speed versus distance in upstream and downstream directions. The bitrate can be varied in steps of 32 kbits/s.

Software

The PC software installation package consists of the NDIS Miniport Drivers and the Hardware Abstraction Layer (HAL) software, which together implement the Microsoft NDIS interface to AAL5, SAR for low-level interfacing to the PCI physical layer. The drivers provide support for peak cell rate upstream traffic shaping. They also operate the ADSL device control panel interface to allow hardware configuration, gathering of statistics, and diagnostic testing.

Chipset Functions

The functions performed by each IC are as follows:

MTC-20154

This CMOS IC contains the analog functions required in the transceiver.

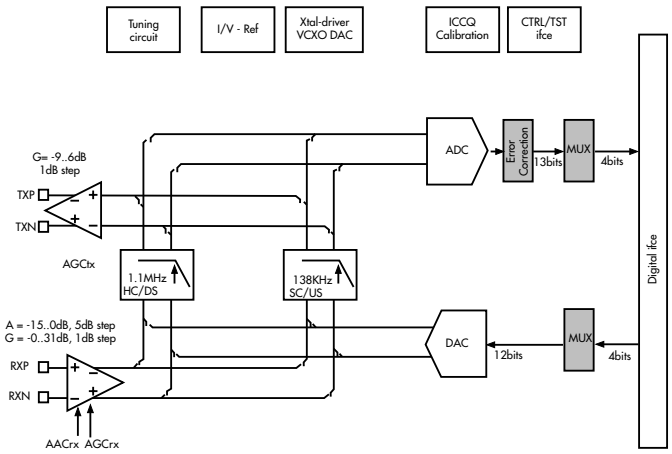

Fig.2: MTC-20154 Block Diagram

In order to cope with the high attenuation of the line and in order to keep acceptable noise level of the signal, automatic gain control amplifiers have been implemented at the analog front of the transmission and reception paths. Then, the signal is passed through low pass filters to eliminate the echo signal and out-of-band interferences.
The AD and DA converters provide 12 bit resolution at 8.8 MHz sampling rate.
Finally, for the transmission part, the control of the external hybrid drivers is done by an integrated highly linear line pre-driver.

MTK-20141

MTC-20147

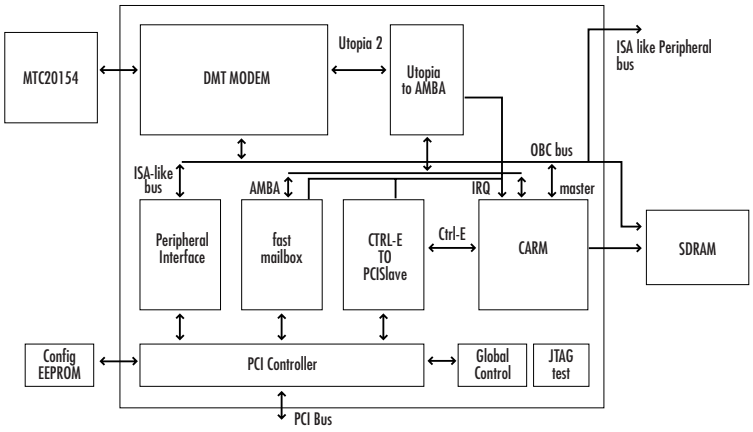

Fig.3: Block Diagram of MTC-20147

1. Discrete Multi Tone (DMT) Modulation and Demodulation

The MTC-20147 implements digitally the Quadrature-Amplitude Modulation (QAM) mapper/demapper which allows up to 14 bits coding per tone (a constellation of 16383 points).
The device implements the necessary Inverse- and Fast Fourier Transform (IFFT, FFT), the Time- and Frequency-Domain Equalizer (TEQ, FEQ) plus timing units and voltage controlled Xtal oscillator (VCXO).
These last blocks implement efficient synchronization algorithms to improve the efficiency of the recovery of data.

2. Framing Functions

The MTC-20147 implements framing functions for the generic and ATM Transmission Convergence (TC) layers. The generic TC consists of data scrambling and Reed-Solomon error correction with and without interleaving.
The ATM TC includes cell level functions (such as cell delineation, insertion/extraction of idle cells, payload scrambling, HEC check) and data frame generation.
Several framing variants are implemented (such as interleaved and non-interleaved modes, full and reduced overhead) to ensure compliance with ANSI T1.413 Issue 2 and ITU G-dmt and G-Lite.

3. PCI Controller

The PCI controller handles all access to PCI configuration space and has a simple FIFO based interface to the application for master and target accesses. The configuration space of the PCI controller uses one BAR to map all memory space addresses in the PC system memory. No addresses are mapped in IO space.
The controller contains the PCI core and some decode logic that routes target accesses to the correct target block. The hard-coded configuration data can be overridden by connecting an external serial EEPROM.

4. Control of Transceiver Chip

The MTC-20147 runs the firmware controlling the operations of the ADSL transceiver (AFE, DMT modem, Framer). During modem initialization, the controller computes and sets up parameters for all programmable DMT functions, filters and equalizers. The controller is able to run in different rate-adaptive modes as defined by the operator.
During operation, the MTC-20147 performs continuous line monitoring and initiates consecutive actions as specified by the operator (e.g. bit-swapping, dynamic bit-rate adaptation, fast retrain...) and collects performance and error information for use by management entities.

5. Interface to Management Entities

The MTC-20147 also runs the communication protocol to interface with external management entities.
A specific ADSL modem control interface has been defined to ease the integration with both systems hardware and firmware. In the MTC-20147 this is accessed via the PCI bus.
This control communication channel is used to transfer information and commands between modem and management entities. These commands/responses can be categorized as follows:

- Configuration of a modem line
- De-allocation of a modem line
- Operational Data Retrieval
- Performance Data Retrieval
- Defect Retrieval

MTK-20141

Table 1: Summary of Characteristics ADSL Chips

MTC-20154

- 4.3 kHz tone spacing
- ADC 12 bit resolution, 8.832 MHz sampling rate
- DAC 12 bit resolution, 8.832 MHz sampling rate
- Analog/tunable low-pass filters
  Upstream channel fc 160 kHz, < 0,2 dB ripple
  Downstream channel fc 1550 kHz, < 1 dB ripple
- AGC range:
  - 15..31 dB in steps of 1 dB (Rx)
  - 9..6 dB in steps of 1 dB (Tx predriver)
- Package: 64 TQFP

MTC-20147

- DMT modulation
  max. number of bit per tone: 14 bits (16383 constellation points)
  max. number of tones: 256 tones
- Max. clock speed: 36 MHz
- Max. tone spacing: 4.325 kHz
- RS encoder: max codeword 256 bytes
- ATM Processor:
  ATM cell buffering
  Cell counting
  Insert/Extract, Idle/Unassigned ATM cells (rate adaptation)
  ATM HEC generation module (CCITT I.432)
  ATM payload scrambler: payload width: 48 bytes
- PCI Interface
- Embedded ARM microcore
- Modem Command interface
  Access through PCI and software API
- Packages: TQFP 176

Table 2: Performance Measurements

Distances	Data rate at 6 dB margin	
0.5 mm 24 AWG	**Upstream**	**Downstream**
0.9 km - 3 kft	820 kbit/s	8 Mbit/s
2.7 km - 9 kft	820 kbit/s	7 Mbit/s
3.6 km - 12 kft	820 kbit/s	5.2 Mbit/s
4.5 km - 15 kft	768 kbit/s	3.2 Mbit/s
6.3 km - 21 kft	640 kbit/s	800 kbit/s

Building Systems with MTK-20141

Great care has been taken in defining the MTK-20141 to ease its integration into system designs. In particular, this is achieved:

- at hardware level: by using standard interfaces both for data transfer (PCI) and for control (PCI or 8-bit parallel/serial)

- at firmware level: by clearly separating the modem firmware, run on the embedded Transceiver Controller from other systems related and application-specific functions. The boundary between the two domains is provided by means of a simple modem control protocol (CTRLE).

- at host environment level: by providing PC miniport drivers and installation software.

This "packaged modem" approach provides a self-contained ADSL modem solution, allowing system manufacturers to concentrate on system issues.

The MTK-20141 comes in a package with full firmware, schematics, Bill of Materials and layout information for the ADSL modem part.
It is further supported by a full development environment comprising:

- Evaluation boards
- PC firmware driver for control port
- PC miniport drivers (NDIS 4.0/5.0) and installation software
- ADSL test and control FW running on PC

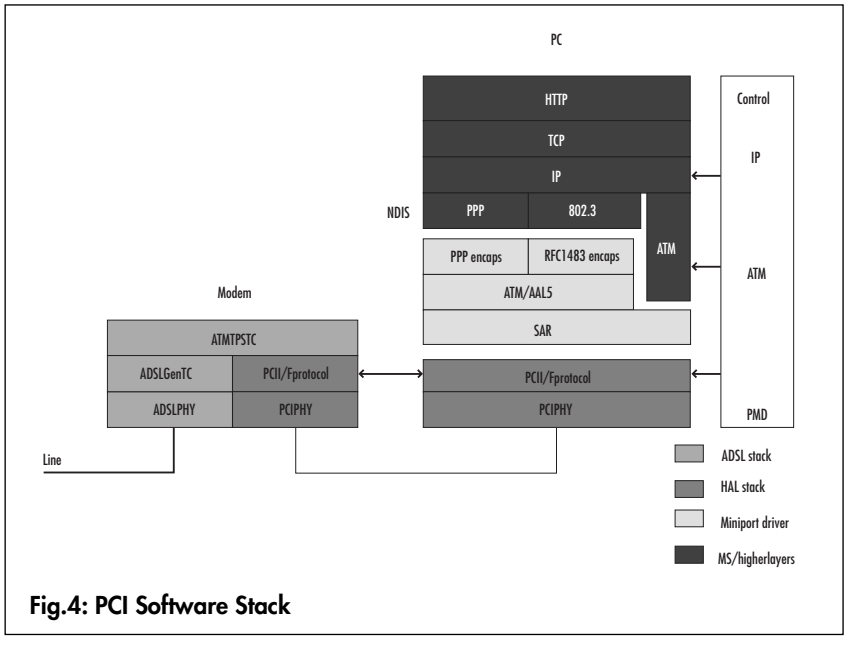

Fig.4: PCI Software Stack

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