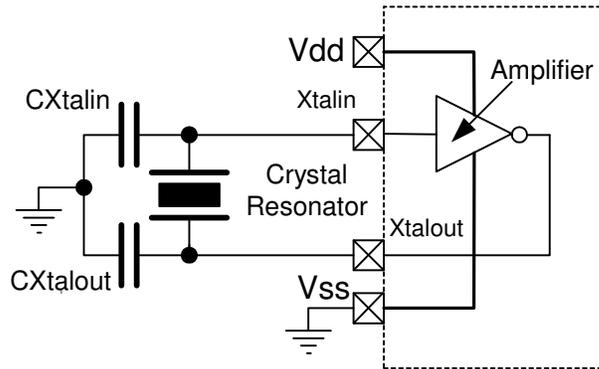


AVR186: Best Practices for the PCB layout of Oscillators

1. Introduction

The Pierce oscillator (most common case) implemented in microcontrollers is built up around a class A amplifier and a narrow band filter such as a crystal or a ceramic resonator as shown in [Figure 1-1](#).

Figure 1-1. Typical Crystal/Resonator Oscillator.



This device has a high input impedance characteristic outside of the resonance frequency range and has a low input impedance characteristic at the oscillation frequency. The high impedance characteristic degrades its immunity when an electrical field is applied in its vicinity. Furthermore, in the latest technology and also in order to reduce the consumption, the oscillation level is restricted to within the range of 1 volt, again increasing the susceptibility.



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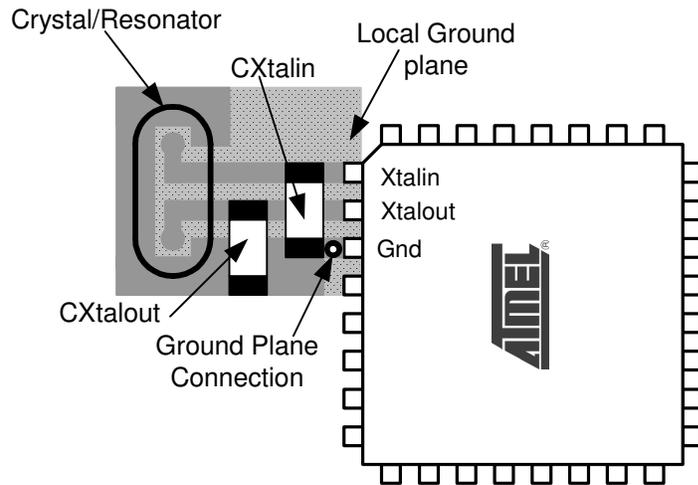
Microcontrollers



2. Description

In order to increase the robustness of this device against external disturbances, the design of the PCB lay-out has to be done very carefully. An example is shown in [Figure 2-1](#).

Figure 2-1. Example of PCB layout.



3. Design Guidelines

The following guidelines to design the layout are highly recommended in order not to risk failure and unstable oscillator operation.

- The crystal and ceramic resonator oscillator is sensitive to stray capacitance and noise from other signals. It should be placed away from high frequency devices and traces in order to reduce the capacitive coupling between Xtal pins and PCB traces.
- Keep other digital signal lines, especially clock lines and frequently switching signal lines, as far as away from the crystal connections as possible. Crosstalk from the digital activities may disturb the small-amplitude sine-shaped oscillator signal.
- The ground connection for the load capacitors should be short and avoid the return currents from USB, RS232, LIN, PWM,... and power lines.
- Load capacitors should be low leakage and stable across temperature (NPO or COG type).
- The load capacitors should be placed close to each other.
- The load Xtal_{in} capacitor should be placed first and closest to the Xtal_{in} pin and ground.
- Parasitic capacitance will reduce gain margin. Keep this to an absolute minimum. For example typically:
 - Xtal_{in} to ground : 1pF
 - Xtal_{out} to ground : 2pF
 - Xtal_{in} to Xtal_{out} : 0.5pF

These values are slightly package dependant.

- Reduce the parasitic capacitance between Xtal_{in} and Xtal_{out} pins by routing them as far apart as possible.
- A ground area should be placed under the crystal oscillator area. This ground land should be connected to the oscillator ground.
-
- Connect the external capacitors needed for the crystal and the ceramic resonator operation as well as the crystal housing to the ground plane.
- In case there is only one PCB layer, it is recommended to place a guard ring around the oscillator components and to connect it to the oscillator ground pin.



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