Integrated Circuit Systems, Inc.

ICS951104
Preliminary Product Preview

Programmable Timing Control Hub™ for P4™

Recommended Application:

ALI 1671/1672 P4 Chipset

Output Features:

- 2 - Pairs of differential CPU clocks (differential current mode)
- 2 - AGP @ 3.3V
- 7 - PCI @ 3.3V
- 1 - 48MHz @ 3.3V fixed
- 1 - REF @ 3.3V, 14.318MHz
- 7 - Pairs of differential SSTL2 DDR @ 2.5V

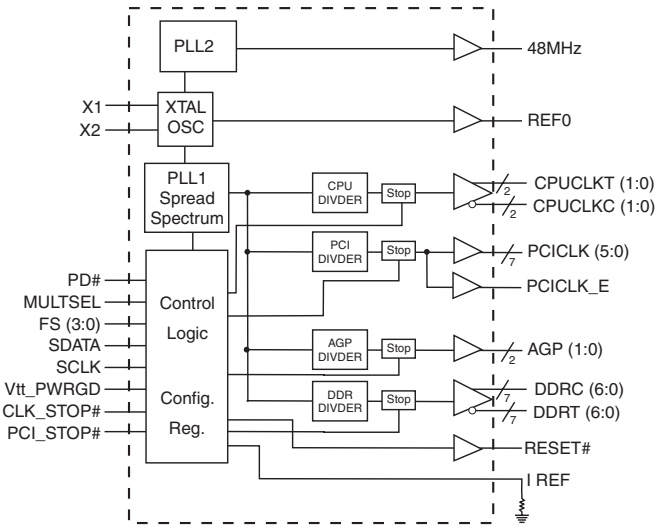
Features/Benefits:

- Programmable output frequency.
- Programmable output divider ratios.
- Programmable output rise/fall time.
- Programmable output skew.
- Programmable spread percentage for EMI control.
- Watchdog timer technology to reset system if system malfunctions.
- Programmable watch dog safe frequency.
- Support I^2C Index read/write and block read/write operations.
- Uses external 14.318MHz crystal.

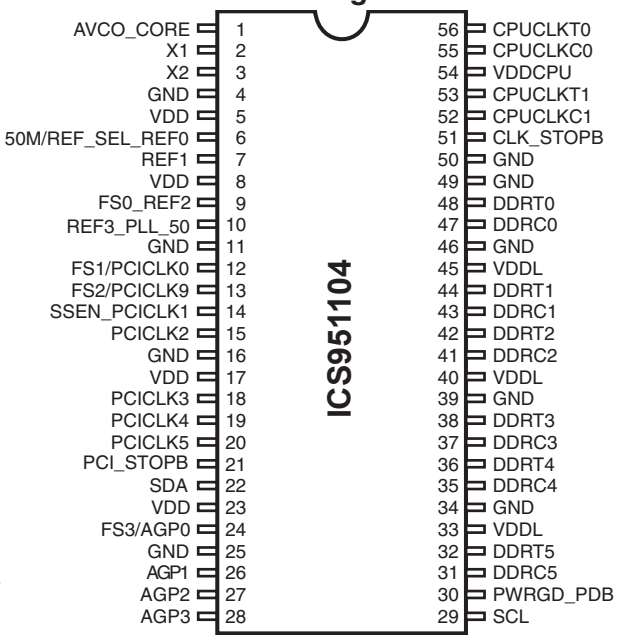
Key Specifications:

- CPU Output Jitter <150ps
- AGP Output Jitter <250ps
- DDR Output Jitter <250ps
- CPU - DDR Skew <250ps
- CPU - AGP/PCI Skew = 2.5ns ± 500ps

Block Diagram



Pin Configuration



56-Pin 300-mil SSOP, 240-mil TSSOP

1 These outputs have 2x drive strength

* Internal Pull-up resistor of 120K to VDD

** These inputs have 120K internal pull-down to GND

Functionality

FS3	FS2	FS1	FS0	CPU	DDR	AGP
0	0	0	0	66.66	66.66	66.66
0	0	0	1	66.66	100.00	66.66
0	0	1	0	100.00	66.66	66.66
0	0	1	1	100.00	100.00	66.66
0	1	0	0	100.00	133.33	66.66
0	1	0	1	133.33	66.66	66.66
0	1	1	0	133.33	100.00	66.66
0	1	1	1	133.33	133.33	66.66
1	0	0	0	66.66	66.66	66.66
1	0	0	1	66.66	100.00	66.66
1	0	1	0	100.00	66.66	66.66
1	0	1	1	100.00	100.00	66.66
1	1	0	0	100.00	133.33	66.66
1	1	0	1	133.33	66.66	66.66
1	1	1	0	133.33	100.00	66.66
1	1	1	1	133.33	133.33	66.66

Host Swing Select Functions

MULTISEL0	Board Target Trace/Term Z	Reference R, Iref = $V_{DD}/(3*Rr)$	Output Current	Voh @ Z
0	50 ohms	Rr = 221 1%, Iref = 5.00mA	Ioh = 4* I REF	1.0V @ 50
1	50 ohms	Rr = 475 1%, Iref = 2.32mA	Ioh = 6* I REF	0.7V @ 50

General Description

The **ICS951104** is a single chip clock solution for desktop designs using the ALI 1671/1672 P4 Chipset. It provides all necessary clock signals for such a system.

The **ICS951104** is part of a whole new line of ICS clock generators and buffers called TCH™ (Timing Control Hub). This part incorporates ICS's newest clock technology which offers more robust features and functionality. Employing the use of a serially programmable I^2C interface, this device can adjust the output clocks by configuring the frequency setting, the output divider ratios, selecting the ideal spread percentage, the output skew, the output strength, and enabling/disabling each individual output clock. M/N control can configure output frequency with resolution up to 0.1MHz increment.

Pin Description

PIN NUMBER	PIN NAME	TYPE	DESCRIPTION
1	AVDD_CORE	PWR	Analog core supply 3.3V
5, 8, 17, 54	VDD	PWR	3.3V power supply.
2	X1	IN	Crystal input, has internal load cap (33pF) and feedback resistor from X2.
3	X2	OUT	Crystal output, nominally 14.318MHz. Has internal load cap (33pF).
4, 11, 16, 25, 34, 39, 46, 49, 50	GND	PWR	Ground pins for 3.3V supply.
6	MULTSEL	IN	3.3V LVTTL input for selecting the current multiplier for CPU outputs
	REF0	OUT	3.3V, 14.318MHz reference clock output.
7	RESET#	OUT	Real time system reset signal for frequency value or watchdog timmer timeout. This signal is active low.
9	FS0	IN	Logic input frequency select bit. Input latched at power on.
	AGP0	OUT	3.3V clock outputs
10	AGP1	OUT	3.3V clock outputs
12	PCICLK_E	OUT	3.3V Early PCI clock output.
	FS1	IN	Logic input frequency select bit. Input latched at power on.
13	FS2	IN	Logic input frequency select bit. Input latched at power on.
	PCICLK0	OUT	3.3V PCI clock output.
20 , 19, 18, 15, 14	PCICLK (5:1)	OUT	3.3V PCI clock outputs.
21	PCI_STOP#	IN	Stops all PCICLKs at logic 0 level, when input low besides the PCICLK_F clocks which are controllable by I2C bits whether they are free running or stopped by PCI_STOP.
22	Vtt_PWRGD	IN	This 3.3V LVTTL input is a level sensitive strobe used to determine when FS (3:0) inputs are valid and are ready to be sampled (active high).
	PD#	IN	Asynchronous active low input pin used to power down the device into a low power state. The internal clocks are disabled and the VCO and the crystal are stopped. The latency of the power down will not be greater than 3ms.
23	AVDD48	PWR	Analog power for 48MHz output 3.3V.
24	FS3	IN	Logic input frequency select bit. Input latched at power on.
	48MHz	OUT	3.3V Fixed 48MHz clock output
26	SDATA	IN	Data pin for I^2C circuitry 5V tolerant.
27	SCLK	I/O	Clock pin for I^2C circuitry 5V tolerant.
28	CLK_STOP#	IN	This asynchronous input halts CPU, AGP or DDR clocks at logic "0" level when driven low. These stops are configurable via IIC.
29, 31, 35, 37, 41, 43, 47	DDRC (6:0)	OUT	"Complementory" clocks of differential pair DDRC outputs.
30, 32, 36, 38, 42, 44, 48	DDRT (6:0)	OUT	"True" clocks of differential pair DDRT outputs.
33, 40, 45	VDDL	PWR	Power supply for 2.5V
51	I REF	OUT	This pin establishes the reference current for the CPUCLK pairs. This pin requires a fixed precision resistor tied to ground in order to establish the appropriate current.
53, 56	CPUCLKT (1:0)	OUT	"True" clocks of differential pair CPU outputs. These are current outputs and external resistors are required for voltage bias.
52, 55	CPUCLKC (1:0)	OUT	"Complementory" clocks of differential pair CPU outputs. These are current outputs and external resistors are required for voltage bias.

General I²C serial interface information

How to Write:

- Controller (host) sends a start bit.
- Controller (host) sends the write address D2 (H)
- ICS clock will ***acknowledge***
- Controller (host) sends the begining byte location = N
- ICS clock will ***acknowledge***
- Controller (host) sends the data byte count = X
- ICS clock will ***acknowledge***
- Controller (host) starts sending ***Byte N through Byte N + X -1***
  (see Note 2)
- ICS clock will ***acknowledge*** each byte ***one at a time***
- Controller (host) sends a Stop bit

Index Block Write Operation			
Controller (Host)			**ICS (Slave/Receiver)**
T	starT bit		
Slave Address D2(H)			
WR	WRite		
			ACK
Beginning Byte = N			
			ACK
Data Byte Count = X			
			ACK
Beginning Byte N		X Byte	
			ACK
	O		
	O		O
	O		O
			O
Byte N + X - 1			
			ACK
P	stoP bit		

How to Read:

- Controller (host) will send start bit.
- Controller (host) sends the write address D2 (H)
- ICS clock will ***acknowledge***
- Controller (host) sends the begining byte location = N
- ICS clock will ***acknowledge***
- Controller (host) will send a separate start bit.
- Controller (host) sends the read address D3 (H)
- ICS clock will ***acknowledge***
- ICS clock will send the data byte count = X
- ICS clock sends ***Byte N + X -1***
- ICS clock sends ***Byte 0 through byte X (if X(H) was written to byte 8)***.
- Controller (host) will need to acknowledge each byte
- Controllor (host) will send a not acknowledge bit
- Controller (host) will send a stop bit

Index Block Read Operation			
Controller (Host)			**ICS (Slave/Receiver)**
T	starT bit		
Slave Address D2(H)			
WR	WRite		
			ACK
Beginning Byte = N			
			ACK
RT	Repeat starT		
Slave Address D3(H)			
RD	ReaD		
			ACK
			Data Byte Count = X
ACK			
		X Byte	Beginning Byte N
ACK			
			O
	O		O
	O		O
	O		
			Byte N + X - 1
N	Not acknowledge		
P	stoP bit		

*See notes on the following page.

Serial Configuration Command Bitmap

Byte0: Functionality and Frequency Select Register (default = 0)

Bit	Description										PWD
		FS3	FS2	FS1	FS0	CPUCLK	DDR	AGP	PCICLK	Spread Precentage	
	Bit2	Bit7	Bit6	Bit5	Bit4	(MHz)	(MHz)	(MHz)	(MHz)		
Bit 2, Bit 7:4	0	0	0	0	0	66.66	66.66	66.66	33.33	+/- 0.25% Center Spread	00000 Note1
	0	0	0	0	1	66.66	100.00	66.66	33.33	+/- 0.25% Center Spread	
	0	0	0	1	0	100.00	66.66	66.66	33.33	+/- 0.25% Center Spread	
	0	0	0	1	1	100.00	100.00	66.66	33.33	+/- 0.25% Center Spread	
	0	0	1	0	0	100.00	133.33	66.66	33.33	+/- 0.25% Center Spread	
	0	0	1	0	1	133.33	66.66	66.66	33.33	+/- 0.25% Center Spread	
	0	0	1	1	0	133.33	100.00	66.66	33.33	+/- 0.25% Center Spread	
	0	0	1	1	1	133.33	133.33	66.66	33.33	+/- 0.25% Center Spread	
	0	1	0	0	0	66.66	66.66	66.66	33.33	0 to -0.5% Down Spread	
	0	1	0	0	1	66.66	100.00	66.66	33.33	0 to -0.5% Down Spread	
	0	1	0	1	0	100.00	66.66	66.66	33.33	0 to -0.5% Down Spread	
	0	1	0	1	1	100.00	100.00	66.66	33.33	0 to -0.5% Down Spread	
	0	1	1	0	0	100.00	133.33	66.66	33.33	0 to -0.5% Down Spread	
	0	1	1	0	1	133.33	66.66	66.66	33.33	0 to -0.5% Down Spread	
	0	1	1	1	0	133.33	100.00	66.66	33.33	0 to -0.5% Down Spread	
	0	1	1	1	1	133.33	133.33	66.66	33.33	0 to -0.5% Down Spread	
	1	0	0	0	0	70.00	70.00	70.00	35.00	+/- 0.25% Center Spread	
	1	0	0	0	1	100.00	166.67	62.50	31.25	+/- 0.25% Center Spread	
	1	0	0	1	0	105.00	70.00	70.00	35.00	+/- 0.25% Center Spread	
	1	0	0	1	1	105.00	105.00	70.00	35.00	+/- 0.25% Center Spread	
	1	0	1	0	0	105.00	140.00	70.00	35.00	+/- 0.25% Center Spread	
	1	0	1	0	1	100.00	166.67	71.43	35.72	+/- 0.25% Center Spread	
	1	0	1	1	0	140.00	105.00	70.00	35.00	+/- 0.25% Center Spread	
	1	0	1	1	1	140.00	140.00	70.00	35.00	+/- 0.25% Center Spread	
	1	1	0	0	0	133.30	166.60	33.33	66.65	Spread Off	
	1	1	0	0	1	73.33	110.00	73.33	36.66	+/- 0.25% Center Spread	
	1	1	0	1	0	110.00	73.33	73.33	36.66	+/- 0.25% Center Spread	
	1	1	0	1	1	110.00	110.00	73.33	36.66	+/- 0.25% Center Spread	
	1	1	1	0	0	110.00	146.66	73.33	36.66	+/- 0.25% Center Spread	
	1	1	1	0	1	146.66	73.33	73.33	36.66	+/- 0.25% Center Spread	
	1	1	1	1	0	146.66	110.00	73.33	36.66	+/- 0.25% Center Spread	
	1	1	1	1	1	146.66	146.66	73.33	36.66	+/- 0.25% Center Spread	
Bit 3	0 - Frequency is selected by hardware select, Latched Inputs 1 - Frequency is selected by Bit 2, 7:4										0
Bit 1	0 - Normal 1 - Spread Spectrum Enabled										0
Bit 0	0 - Running 1- Tristate all outputs										0

Note1: Default at power-up will be for latched logic inputs to define frequency, as displayed by Bit 3.
The I^2C readback of the power up default indicates the revision ID in bits 2, 7:4 as shown.

Byte 1: Output Control Register
(1 = enable, 0 = disable)

Bit	Pin#	PWD	Description
Bit7	-	X	MULT_SEL (readback)
Bit6	53, 52	1	CPUT/C1
Bit5	56, 55	1	CPUT/C0
Bit4	20	1	PCICLK_5 drive strength control 1 = 2X, 0 = 1X
Bit3	-	X	FS3 Read back
Bit2	-	X	FS2 Read back
Bit1	-	X	FS1 Read back
Bit0	-	X	FS0 Read back

Byte 2: Output Control Register
(1 = enable, 0 = disable)

Bit	Pin#	PWD	Description
Bit7	12	1	PCICLK_E
Bit6	20	1	PCICLK_5
Bit5			
Bit4	19	1	PCICLK_4
Bit3	18	1	PCICLK_3
Bit2	15	1	PCICLK_2
Bit1	14	1	PCICLK_1
Bit0	13	1	PCICLK_0

Byte 3: Output Control Register
(1 = enable, 0 = disable)

Bit	Pin#	PWD	Description
Bit7	24	1	48MHZ
Bit6	48, 47	1	DDRT/C0
Bit5	-	1	Reset gear shift detect 1 = Enable, 0 = Disable
Bit4	42, 41, 44, 43	1	DDRT/C (2:1)
Bit3	36, 35, 38, 37	1	DDRT/C (4:3)
Bit2	30, 29, 32, 31	1	DDRT/C (6:5)
Bit1	10	1	AGP1
Bit0	9	1	AGP0

Byte 4: Output Control Register
(1 = enable, 0 = disable)

Bit	Pin#	PWD	Description
Bit 7	-	0	CPUT/C0 Stop via CLK_STOP enable bit, 0 = Free Run; 1 = Stoppable
Bit 6	-	0	CPUT/C1 Stop via CLK_STOP enable bit, 0 = Free Run; 1 = Stoppable
Bit 5	-	0	AGP0 Stop via CLK_STOP enable bit, 0 = Free Run; 1 = Stoppable
Bit 4	-	0	AGP1 Stop via CLK_STOP enable bit, 0 = Free Run; 1 = Stoppable
Bit 3	-	0	DDRT/C(6:0) Stop via CLK_STOP enable bit, 0 = Free Run; 1 = Stoppable
Bit 2	-	0	DDRT/C0 Stop via CLK_STOP enable bit, 0 = Free Run; 1 = Stoppable
Bit 1	-	0	CPUCLKT1 PD# STOP polarity control, 0 = Stop High; 1 = Stop Low
Bit 0	-	0	CPUCLKT0 PD# STOP polarity control, 0 = Stop High; 1 = Stop Low

Byte 5: Programming Edge Rate
(1 = enable, 0 = disable)

Bit	Pin#	PWD	Description
Bit 7	X	0	PCICLK_E STOP via PCI_STOP enable bit, 0 = Free Run; 1 = Stoppable
Bit 6	X	0	PCICLK5 STOP via PCI_STOP enable bit, 0 = Free Run; 1 = Stoppable
Bit 5			
Bit 4	X	0	PCICLK4 STOP via PCI_STOP enable bit, 0 = Free Run; 1 = Stoppable
Bit 3	X	0	PCICLK3 STOP via PCI_STOP enable bit, 0 = Free Run; 1 = Stoppable
Bit 2	X	0	PCICLK2 STOP via PCI_STOP enable bit, 0 = Free Run; 1 = Stoppable
Bit 1	X	0	PCICLK1 STOP via PCI_STOP enable bit, 0 = Free Run; 1 = Stoppable
Bit 0	X	0	PCICLK0 STOP via PCI_STOP enable bit, 0 = Free Run; 1 = Stoppable

Byte 6: Vendor ID Register
(1 = enable, 0 = disable)

Bit	Name	PWD	Description
Bit 7	Revision ID Bit3	X	Revision ID values will be based on individual device's revision
Bit 6	Revision ID Bit2	X	
Bit 5	Revision ID Bit1	X	
Bit 4	Revision ID Bit0	X	
Bit 3	Vendor ID Bit3	0	(Reserved)
Bit 2	Vendor ID Bit2	0	(Reserved)
Bit 1	Vendor ID Bit1	0	(Reserved)
Bit 0	Vendor ID Bit0	1	(Reserved)

Byte 7: Revision ID and Device ID Register

Bit	Name	PWD	Description
Bit 7	Device ID7	0	Device ID values will be based on individual device "22H" in this case.
Bit 6	Device ID6	0	
Bit 5	Device ID5	1	
Bit 4	Device ID4	0	
Bit 3	Device ID3	0	
Bit 2	Device ID2	0	
Bit 1	Device ID1	1	
Bit 0	Device ID0	0	

Byte 8: Byte Count Read Back Register

Bit	Name	PWD	Description
Bit 7	Byte7	0	Note: Writing to this register will configure byte count and how many bytes will be read back, default is $0F_H$ = 15 bytes.
Bit 6	Byte6	0	
Bit 5	Byte5	0	
Bit 4	Byte4	0	
Bit 3	Byte3	1	
Bit 2	Byte2	1	
Bit 1	Byte1	1	
Bit 0	Byte0	1	

Byte 9: Watchdog Timer Count Register

Bit	Name	PWD	Description
Bit 7	WD7	0	The decimal representation of these 8 bits correspond to X • 290ms the watchdog timer will wait before it goes to alarm mode and reset the frequency to the safe setting. Default at power up is 8 • 290ms = 2.3 seconds.
Bit 6	WD6	0	
Bit 5	WD5	0	
Bit 4	WD4	0	
Bit 3	WD3	1	
Bit 2	WD2	0	
Bit 1	WD1	0	
Bit 0	WD0	0	

Byte 10: Programming Enable bit 8 Watchdog Control Register

Bit	Name	PWD	Description
Bit 7	Program Enable	0	Programming Enable bit 0 = no programming. Frequencies are selected by HW latches or Byte0 1 = enable all I²C programing.
Bit 6	WD Enable	0	Watchdog Enable bit. This bit will over write WDEN latched value. 0 = disable, 1 = Enable.
Bit 5	WD Alarm	0	Watchdog Alarm Status 0 = normal 1= alarm status
Bit 4	SF4	0	Watchdog safe frequency bits. Writing to these bits will configure the safe frequency corrsponding to Byte 0 Bit 2, 7:4 table
Bit 3	SF3	0	
Bit 2	SF2	0	
Bit 1	SF1	0	
Bit 0	SF0	0	

Byte 11: VCO Frequency M Divider (Reference divider) Control Register

Bit	Name	PWD	Description
Bit 7	Ndiv 8	X	N divider bit 8
Bit 6	Mdiv 6	X	The decimal respresentation of Mdiv (6:0) corresposd to the reference divider value. Default at power up is equal to the latched inputs selection.
Bit 5	Mdiv 5	X	
Bit 4	Mdiv 4	X	
Bit 3	Mdiv 3	X	
Bit 2	Mdiv 2	X	
Bit 1	Mdiv 1	X	
Bit 0	Mdiv 0	X	

Byte 12: VCO Frequency N Divider (VCO divider) Control Register

Bit	Name	PWD	Description
Bit 7	Ndiv 7	X	The decimal representation of Ndiv (8:0) correspond to the VCO divider value. Default at power up is equal to the latched inputs selecton. Notice Ndiv 8 is located in Byte 11.
Bit 6	Ndiv 6	X	
Bit 5	Ndiv 5	X	
Bit 4	Ndiv 4	X	
Bit 3	Ndiv 3	X	
Bit 2	Ndiv 2	X	
Bit 1	Ndiv 1	X	
Bit 0	Ndiv 0	X	

Byte 13: Spread Spectrum Control Register

Bit	Name	PWD	Description
Bit 7	SS 7	X	The Spread Spectrum (12:0) (or, see Byte 14) bit will program the spread precentage. Spread precent needs to be calculated based on the VCO frequency, spreading profile, spreading amount and spread frequency. It is recommended to use ICS software for spread programming. Default power on is latched FS divider.
Bit 6	SS 6	X	
Bit 5	SS 5	X	
Bit 4	SS 4	X	
Bit 3	SS 3	X	
Bit 2	SS 2	X	
Bit 1	SS 1	X	
Bit 0	SS 0	X	

Byte 14: Spread Spectrum Control Register

Bit	Name	PWD	Description
Bit 7	Reserved	X	Reserved
Bit 6	Reserved	X	Reserved
Bit 5	Reserved	X	Reserved
Bit 4	SS 12	X	Spread Spectrum Bit 12
Bit 3	SS 11	X	Spread Spectrum Bit 11
Bit 2	SS 10	X	Spread Spectrum Bit 10
Bit 1	SS 9	X	Spread Spectrum Bit 9
Bit 0	SS 8	X	Spread Spectrum Bit 8

Byte 15: Output Divider Control Register

Bit	Name	PWD	Description
Bit 7	DDRC Div 3	X	DDRC clock divider ratio can be configured via these 4 bits individually. For divider selection table refer to Table 1. Default at power up is latched FS divider.
Bit 6	DDRC Div 2	X	
Bit 5	DDRC Div 1	X	
Bit 4	DDRC Div 0	X	
Bit 3	CPU Div 3	X	CPUCLK1 clock divider ratio can be configured via these 4 bits individually. For divider selection table refer to Table 1. Default at power up is latched FS divider.
Bit 2	CPU Div 2	X	
Bit 1	CPU Div 1	X	
Bit 0	CPU Div 0	X	

Byte 16: Output Divider Control Register

Bit	Name	PWD	Description
Bit 7	DDRT Div 3	X	DDRT clock divider ratio can be configured via these 4 bits individually. For divider selection table refer to Table 1. Default at power up is latched FS divider.
Bit 6	DDRT Div 2	X	
Bit 5	DDRT Div 1	X	
Bit 4	DDRT Div 0	X	
Bit 3	AGP Div 3	X	AGP clock divider ratio can be configured via these 4 bits individually. For divider selection table refer to Table 1. Default at power up is latched FS divider.
Bit 2	AGP Div 2	X	
Bit 1	AGP Div 1	X	
Bit 0	AGP Div 0	X	

Byte 17: Output Divider Control Register

Bit	Name	PWD	Description
Bit 7	PCI_INV	X	PCICLK Phase Inversion bit
Bit 6	3V66_INV	X	3V66 Phase Inversion bit
Bit 5	Reserved	X	Reserved
Bit 4	CPU_INV	X	CPUCLK Phase Inversion bit
Bit 3	PCI Div 3	X	PCI clock divider ratio can be configured via these 4 bits individually. For divider selection table refer to Table 2. Default at power up is latched FS divider.
Bit 2	PCI Div 2	X	
Bit 1	PCI Div 1	X	
Bit 0	PCI Div 0	X	

Table 1

Div (3:2) / Div (1:0)	00	01	10	11
00	/2	/4	/8	/16
01	/3	/6	/12	/24
10	/5	/10	/20	/40
11	/7	/14	/28	/56

Table 2

Div (3:2) / Div (1:0)	00	01	10	11
00	/4	/8	/16	/32
01	/3	/6	/12	/24
10	/5	/10	/20	/40
11	/9	/18	/36	/72

Byte 18: Group Skew Control Register

Bit	Name	PWD	Programming Sequence					
Bit 7	These 4bits control CPU-DDRC (6:0)	0	0	0	0	0	0ps	Reserved
Bit 6		0	0	1	0	0	150ps	Reserved
Bit 5		0	1	0	0	0	300ps	Reserved
Bit 4		0	1	1	0	0	450ps	Reserved
Bit 3	These 4 bits control all clocks to CPUT/C (1:0)	1	1	1	0	1	600ps	Reserved
Bit 2		1	1	1	1	0	750ps	Reserved
Bit 1		1	1	1	1	1	900ps	Reserved
Bit 0		1	Reserved					Reserved

Byte 19: Group Skew Control Register

Bit	Name	PWD	CPU-DDR					CPU-AGP								
Bit 7	These 4bits control CPU-DDRT (6:0)	0	0	0	0	0	0ps	0	0	0	0	1.85ns	1	0	0	0	3.05ns
Bit 6		0	0	1	0	0	150ps	0	0	0	1	2.00ns	1	0	0	1	3.20ns
Bit 5		0	1	0	0	0	300ps	0	0	1	0	2.15ns	1	0	1	0	3.35ns
Bit 4		0	1	1	0	0	450ps	0	0	1	1	2.30ns	1	0	1	1	3.50ns
Bit 3	These 4 bits control CPU-AGP(1:0)	1	1	1	0	1	600ps	0	1	0	0	2.45ns	1	1	0	0	3.65ns
Bit 2		1	1	1	1	0	750ps	0	1	0	1	2.60ns	1	1	0	1	3.80ns
Bit 1		0	1	1	1	1	900ps	0	1	1	0	2.75ns	1	1	1	0	3.95ns
Bit 0		1	Reserved					0	1	1	1	2.90ns	1	1	1	1	4.10ns

Byte 20: Group Skew Control Register

Bit	Name	PWD	CPU-PCI_E					CPU-PCI								
Bit 7	These 4bits control CPU-PCI(6:0)	0	0	0	0	0	0ps	0	0	0	0	1.85ns	1	0	0	0	3.05ns
Bit 6		0	0	1	0	0	150ps	0	0	0	1	2.00ns	1	0	0	1	3.20ns
Bit 5		0	1	0	0	0	300ps	0	0	1	0	2.15ns	1	0	1	0	3.35ns
Bit 4		0	1	1	0	0	450ps	0	0	1	1	2.30ns	1	0	1	1	3.50ns
Bit 3	These 4 bits control CPU-PCI_E	1	1	1	0	1	600ps	0	1	0	0	2.45ns	1	1	0	0	3.65ns
Bit 2		0	1	1	1	0	750ps	0	1	0	1	2.60ns	1	1	0	1	3.80ns
Bit 1		0	1	1	1	1	900ps	0	1	1	0	2.75ns	1	1	1	0	3.95ns
Bit 0		0	Reserved					0	1	1	1	2.90ns	1	1	1	1	4.10ns

Byte 21: Slew Rate Control Register

Bit	Name	PWD	Strength Select
Bit 7	REF0	1	Clock slew rate control bits. 01 = strong: 11 = 00 medium: 10 = weak
Bit 6		0	
Bit 5	REF0	1	Select 1X = 1: 2X = 0
Bit 4	Reserved	X	Reserved
Bit 3	AGP(1:0)	1	Clock slew rate control bits. 01 = strong: 11 = 00 medium: 10 = weak
Bit 2		0	
Bit 1	Reserved	X	Reserved
Bit 0		X	

Byte 22: Slew Rate Control Register

Bit	Name	PWD	Strength Select
Bit 7	PCI_E	1	Clock slew rate control bits. 01 = strong: 11 = 00 medium: 10 = weak
Bit 6		0	
Bit 5	PCI5	1	Clock slew rate control bits. 01 = strong: 11 = 00 medium: 10 = weak
Bit 4		0	
Bit 3	PCI(4:2)	1	Clock slew rate control bits. 01 = strong: 11 = 00 medium: 10 = weak
Bit 2		0	
Bit 1	PCI(1:0)	1	Clock slew rate control bits. 01 = strong: 11 = 00 medium: 10 = weak
Bit 0		0	

Byte 23: Slew Rate Control Register

Bit	Name	PWD	Strength Select
Bit 7	Reserved	X	Reserved
Bit 6		X	
Bit 5	Reserved	X	Reserved
Bit 4		X	
Bit 3	Reserved	X	Reserved
Bit 2		X	
Bit 1	48MHz	1	Clock slew rate control bits. 01 = strong: 11 = 00 medium: 10 = weak
Bit 0		0	

Absolute Maximum Ratings

Supply Voltage . . . . . 5.5 V
Logic Inputs . . . . . GND –0.5 V to V_{DD} +0.5 V
Ambient Operating Temperature . . . . . 0°C to +70°C
Case Temperature . . . . . 115°C
Storage Temperature . . . . . –65°C to +150°C

Stresses above those listed under *Absolute Maximum Ratings* may cause permanent damage to the device. These ratings are stress specifications only and functional operation of the device at these or any other conditions above those listed in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect product reliability.

Electrical Characteristics - Input/Supply/Common Output Parameters

T_A = 0 - 70C; Supply Voltage V_{DD} = 3.3 V ±5%

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
Input High Voltage	V_{IH}		2		V_{DD}+0.3	V
Input Low Voltage	V_{IL}		V_{SS}-0.3		0.8	V
Input High Current	I_{IH}	V_{IN} = V_{DD}	-5		5	mA
Input Low Current	I_{IL1}	V_{IN} = 0 V; Inputs with no pull-up resistors	-5			mA
Input Low Current	I_{IL2}	V_{IN} = 0 V; Inputs with pull-up resistors	-200			mA
Operating Supply Current	$I_{DD3.3OP}$	C_L = 0 pF; Select @ 66M			100	mA
		C_L = Full load			280	mA
Power Down Supply Current	$I_{DD3.3PD}$	IREF=2.32			20	mA
		IREF= 5mA			37	mA
Input frequency	F_i	V_{DD} = 3.3 V;				MHz
Pin Inductance	L_{pin}				7	nH
Input Capacitance[1]	C_{IN}	Logic Inputs			5	pF
	C_{out}	Out put pin capacitance			6	pF
	C_{INX}	X1 & X2 pins	27		45	pF
Transition Time[1]	T_{trans}	To 1st crossing of target Freq.			3	mS
Settling Time[1]	T_s	From 1st crossing to 1% target Freq.			3	mS
Clk Stabilization[1]	T_{STAB}	From V_{DD} = 3.3 V to 1% target Freq.			3	mS
Delay	t_{PZH},t_{PZH}	output enable delay (all outputs)	1		10	nS
	t_{PLZ},t_{PZH}	output disable delay (all outputs)	1		10	nS

[1]Guarenteed by design, not 100% tested in production.

Electrical Characteristics - CPUCLKT/C

T_A = 0 - 70º C; V_{DD} = 3.3 V +/-5%; (unless otherwise stated)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
Current Source Output Impedance	Z_O	$V_O = V_X$	3000			W
Output High Voltage	V_{OH}	V_R = 475W ±1%; IREF = 2.32mA; I_{OH} = 6*IREF		0.71	1.2	V
Output High Current	I_{OH}			-13.9		mA
Rise Time[1]	t_r	V_{OL} = 20%, V_{OH} = 80%	175		600	ps
Differential Crossover Voltage[1]	V_X	Note 3	45	50	55	%
Duty Cycle[1]	d_t	V_T = 50%	45	51	55	%
Skew[1], CPU to CPU	t_{sk}	V_T = 50%			100	ps
Jitter, Cycle-to-cycle[1]	$t_{jcyc-cyc}$	$V_T = V_X$			150	ps

Notes:
1 - Guaranteed by design, not 100% tested in production.

Electrical Characteristics - PCICLK

T_A = 0 - 70C; V_{DD} = 3.3 V +/-5%; C_L = 10-30 pF (unless otherwise stated)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
Output Frequency	F0[1]			33.33		MHz
Output Impedance	R_{DSN1}[1]	$V_O = V_{DD}$*(0.5)	12		55	W
Output High Voltage	V_{OH1}	I_{OH} = -1 mA	2.4			V
Output Low Voltage	V_{OL1}	I_{OL} = 1 mA			0.55	V
Output High Current	I_{OH1}	VOH@ MIN = 1.0 V, VOH@ MAX = 3.135 V	-33		-33	mA
Output Low Current	I_{OL1}	VOL@ MIN = 1.95 V, VOL@ MAX= 0.4	30		38	mA
Rise Time	t_{r1}[1]	V_{OL} = 0.4 V, V_{OH} = 2.4 V	0.5		2.5	ns
Fall Time	t_{f1}[1]	V_{OH} = 2.4 V, V_{OL} = 0.4 V	0.5		2.5	ns
Duty Cycle	d_{t1}[1]	V_T = 1.5 V	45		55	%
Skew	t_{sk1}[1]	V_T = 1.5 V			150	ps
Jitter PCI (5:0)	$t_{jcyc-cyc}$[1]	V_T = 1.5 V			350	ps
Jitter PCI_E	$t_{CYC-CYC}$	V_T = 1.5V			200	ps
Skew PCI_E-PCI (5:0)	t_{SK}	V_T = 1.5V	1	3.2	3.5	ns

[1]Guarenteed by design, not 100% tested in production.

Electrical Characteristics - DDRT/C

T_A = 0 - 70º C; V_{DD} = 3.3 V +/-5%, V_{DDL} = 2.5 V +/-5%; C_L = 30 pF (unless otherwise stated)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
Output High Voltage	V_{OH3}	I_{OH} = -28 mA	2.4			V
Output Low Voltage	V_{OL3}	I_{OL} = 23 mA			0.4	V
Output High Current	I_{OH3}	V_{OH} = 2.0 V			-54	mA
Output Low Current	I_{OL3}	V_{OL} = 0.8 V	41			mA
Rise Time	T_{r3}[1]	20-80	450		1200	ps
Fall Time	T_{f3}[1]	80-20	450		1200	ps
Duty Cycle	D_{t3}[1]	V_T = 1.5 V	45		55	%
Jitter		V_T			150	ps
Skew[1]	T_{sk1}	V_T = 1.5 V			150	ps

Electrical Characteristics - AGP

T_A = 0 - 70C; V_{DD} = 3.3 V +/-5%; C_L =10-30 pF (unless otherwise stated)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
Output Frequency	F_{O1}			66.66		MHz
Output Impedance	R_{DSP1}[1]	$V_O = V_{DD}$*(0.5)	12		55	W
Output High Voltage	V_{OH1}	I_{OH} = -1 mA	2.4			V
Output Low Voltage	V_{OL1}	I_{OL} = 1 mA			0.4	V
Output High Current	I_{OH1}	VOH@ MIN = 1.0 V, VOH@ MAX = 3.135 V	-33		-33	mA
Output Low Current	I_{OL1}	VOL@ MIN = 1.95 V, VOL@ MAX= 0.4	30		38	mA
Rise Time	t_{r1}[1]	V_{OL} = 0.4 V, V_{OH} = 2.4 V	0.5		2	ns
Fall Time	t_{f1}[1]	V_{OH} = 2.4 V, V_{OL} = 0.4 V	0.5		2	ns
Duty Cycle	d_{t1}[1]	V_T = 1.5 V	45		55	%
Skew	t_{sk1}[1]	V_T = 1.5 V			100	ps
Jitter	tjcyc-cyc[1]	V_T = 1.5 V			450	ps

[1]Guarenteed by design, not 100% tested in production.

Electrical Characteristics - 48MHz

T_A = 0 - 70C; V_{DD} = 3.3 V +/-5%; C_L = 10-30 pF (unless otherwise stated)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
Output Frequency	F_O[1]	$V_O = V_{DD}*(0.5)$		48		MHz
Output Impedance	R_{DSN1}[1]	$V_O = V_{DD}*(0.5)$	12		55	W
Output High Voltage	V_{OH1}	I_{OH} = -1 mA	2.4			V
Output Low Voltage	V_{OL1}	I_{OL} = 1 mA			0.55	V
Output High Current	I_{OH1}	VOH@ MIN = 1.0 V, VOH@ MAX = 3.135 V	-29		-23	mA
Output Low Current	I_{OL1}	VOL@ MIN = 1.95 V, VOL@ MAX= 0.4	29		27	mA
VCH 48 USB Rise Time	t_r[1]	V_{OL} = 0.4 V, V_{OH} = 2.4 V			1.5	ns
VCH 48 USB Fall Time	tf[1]	V_{OH} = 2.4 V, V_{OL} = 0.4 V			1.5	ns
Duty Cycle	d_{t1}[1]	V_T = 1.5 V	45		55	%
Jitter	$t_{jcyc-cyc}$[1]	V_T = 1.5 V			350	ps

[1]Guarenteed by design, not 100% tested in production.

Electrical Characteristics - REF

T_A = 0 - 70C; VDD=3.3V +/-5%; C_L = 10-20 pF (unless otherwise specified)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
Output Frequency	F_{O1}					MHz
Output Impedance	R_{DSP1}[1]	$V_O = V_{DD}*(0.5)$	20		60	W
Output High Voltage	V_{OH}[1]	I_{OH} = -1 mA	2.4			V
Output Low Voltage	V_{OL}[1]	I_{OL} = 1 mA			0.4	V
Output High Current	I_{OH}[1]	$V_{OH@MIN}$ = 1.0 V, $V_{OH@MAX}$ = 3.135 V	-29		-23	mA
Output Low Current	I_{OL}[1]	$V_{OL@MIN}$ = 1.95 V, $V_{OL@MAX}$ = 0.4 V	29		27	mA
Rise Time	t_{r1}[1]	V_{OL} = 0.4 V, V_{OH} = 2.4 V			2	ns
Fall Time	t_{f1}[1]	V_{OH} = 2.4 V, V_{OL} = 0.4 V			2	ns
Duty Cycle	d_{t1}[1]	V_T = 1.5 V	45		55	%
Jitter	$t_{jcyc-cyc}$[1]	V_T = 1.5 V			1000	ps

[1]Guaranteed by design, not 100% tested in production.

Shared Pin Operation - Input/Output Pins

The I/O pins designated by (input/output) serve as dual signal functions to the device. During initial power-up, they act as input pins. The logic level (voltage) that is present on these pins at this time is read and stored into a 5-bit internal data latch. At the end of Power-On reset, (see AC characteristics for timing values), the device changes the mode of operations for these pins to an output function. In this mode the pins produce the specified buffered clocks to external loads.

To program (load) the internal configuration register for these pins, a resistor is connected to either the VDD (logic 1) power supply or the GND (logic 0) voltage potential. A 10 Kilohm (10K) resistor is used to provide both the solid CMOS programming voltage needed during the power-up programming period and to provide an insignificant load on the output clock during the subsequent operating period.

Figure 1 shows a means of implementing this function when a switch or 2 pin header is used. With no jumper is installed the pin will be pulled high. With the jumper in place the pin will be pulled low. If programmability is not necessary, than only a single resistor is necessary. The programming resistors should be located close to the series termination resistor to minimize the current loop area. It is more important to locate the series termination resistor close to the driver than the programming resistor.

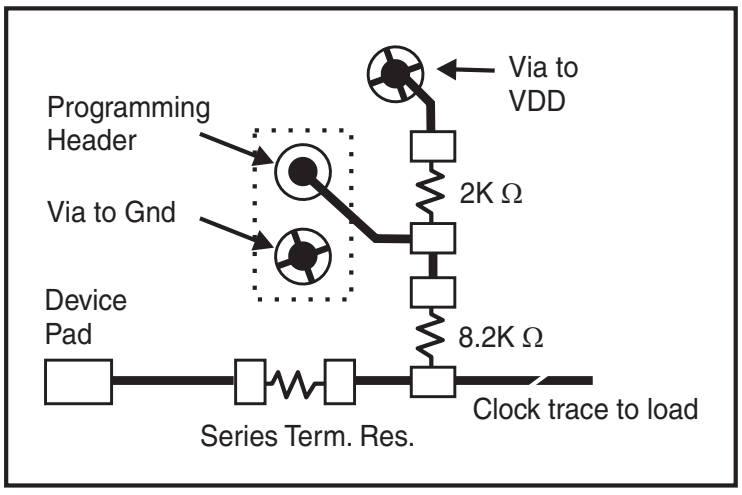
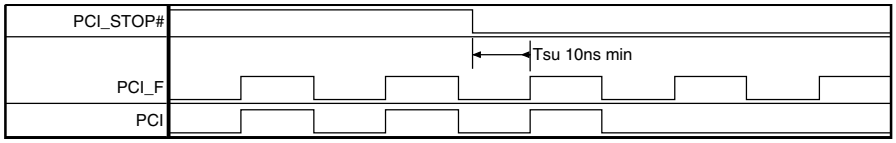


Fig. 1

PCI_STOP# - Assertion (transition from logic "1" to logic "0")

The impact of asserting the PCI_STOP# signal will be the following. All PCI[6:0] and stoppable PCI_F[2,0] clocks will latch low in their next high to low transition. The PCI_STOP# setup time tsu is 10 ns, for transitions to be recognized by the next rising edge.

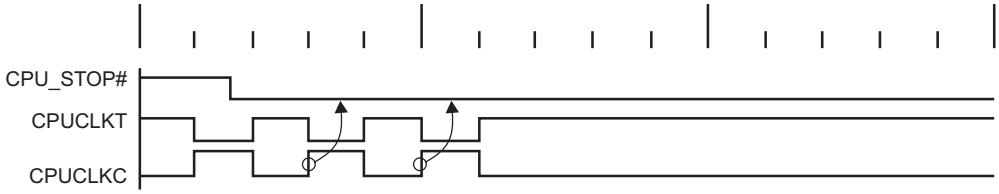
Assertion of PCI_STOP# Waveforms



CPU_STOP# - Assertion (transition from logic "1" to logic "0")

The impact of asserting the CPU_STOP# pin is all CPU outputs that are set in the I^2C configuration to be stoppable via assertion of CPU_STOP# are to be stopped after their next transition. When the I^2C Bit 6 of Byte 1 is programmed to '0' the final state of the stopped CPU signals is CPU = High and CPU# = Low. There is to be no change to the output drive current values. The CPU will be driven high with a current value equal to (Mult 0 'select') x (Iref), the CPU# signal will not be driven . When the I^2C Bit 6 of Byte 1 is programmed to '1' then final state of the stopped CPU signals is Low, both CPU and CPU# outputs will not be driven.

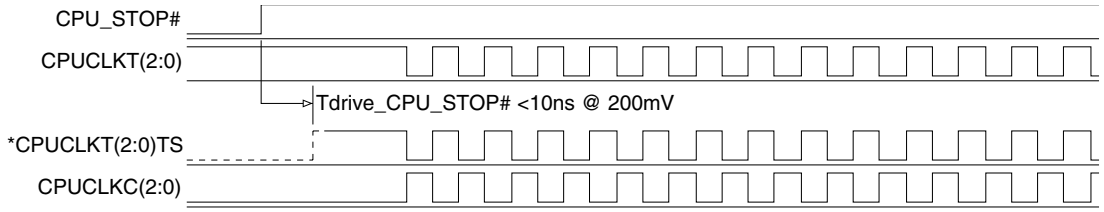
Assertion of CPU_STOP# Waveforms



CPU_STOP# - De-assertion (transition from logic "0" to logic "1")

All CPU outputs that were stopped are to resume normal operation in a glitch free manner. The maximum latency from the de-assertion to active outputs is to be defined to be between 2 - 6 CPU clock periods (2 clocks are shown). If the I2C Bit 6 of Byte 1 is programmed to "1" then the stopped CPU outputs will be driven High within 3 nS of CPU_Stop# de-assertion.

De-assertion of CPU_STOP# Waveforms

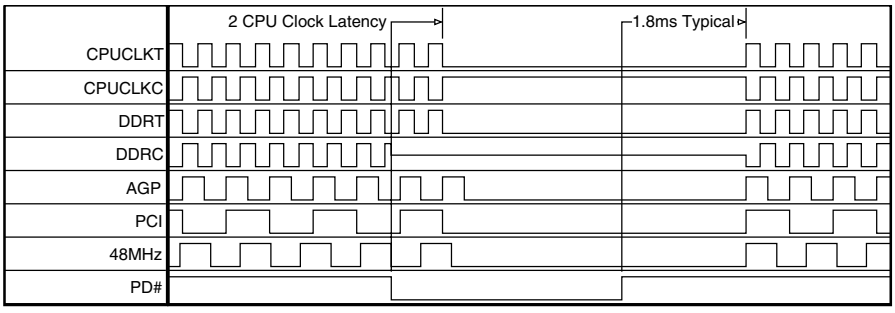


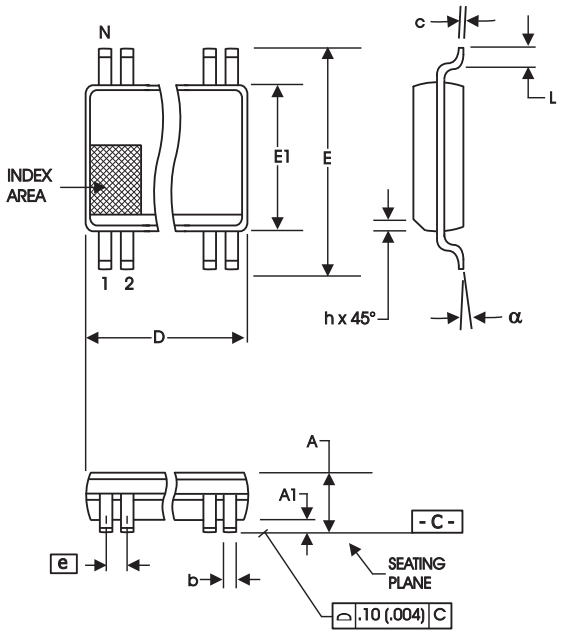
*Signal TS is CPUCLKT in Tri-State mode

PD# - Assertion (transition from logic "1" to logic "0")

When PWRDWN# is sampled low by two consecutive rising edges of CPU clock, then all clock outputs except CPU clocks must be held low on their next high to low transitions. When the I2C Bit 6 of Byte 0 is programmed to '0' CPU clocks must be held with the CPU clock pin driven high with a value of 2 x Iref, and CPU# undriven. If Bit 6 of Byte 0 is '1' then both CPU and CPU# are undriven. Note the example below shows CPU = 133 MHz and Bit 6 of Byte 0 = '0', this diagram and description is applicable for all valid CPU frequencies 66, 100, 133, 200 MHz.
Due to the state if the internal logic, stopping and holding the REF clock outputs in the LOW state may require more than one clock cycle to complete.

Power Down Assertion of Waveforms





300 mil SSOP Package

SYMBOL	In Millimeters COMMON DIMENSIONS		In Inches COMMON DIMENSIONS	
	MIN	MAX	MIN	MAX
A	2.41	2.80	.095	.110
A1	0.20	0.40	.008	.016
b	0.20	0.34	.008	.0135
c	0.13	0.25	.005	.010
D	SEE VARIATIONS		SEE VARIATIONS	
E	10.03	10.68	.395	.420
E1	7.40	7.60	.291	.299
e	0.635 BASIC		0.025 BASIC	
h	0.38	0.64	.015	.025
L	0.50	1.02	.020	.040
N	SEE VARIATIONS		SEE VARIATIONS	
α	0°	8°	0°	8°

VARIATIONS

N	D mm.		D (inch)	
	MIN	MAX	MIN	MAX
56	18.31	18.55	.720	.730

Reference Doc.: JEDEC Publication 95, MO-118

10-0034

Ordering Information

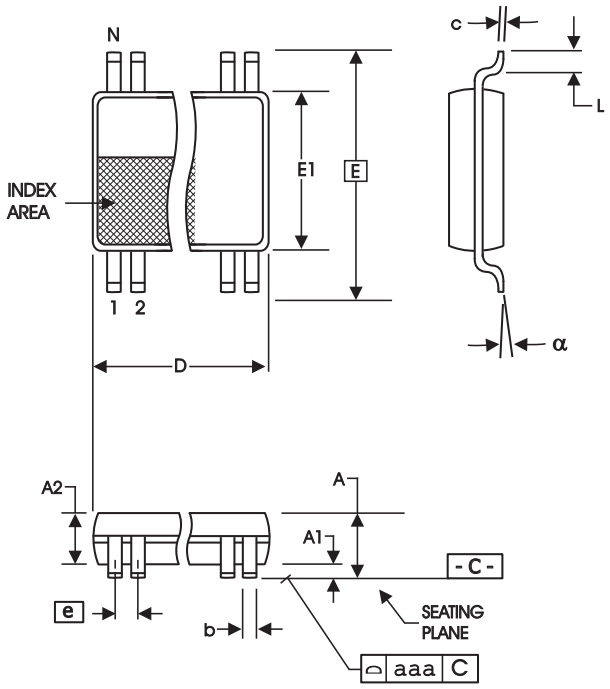
ICS951104yFLFT

Example:

ICS XXXXXX y F LF - T

- **Designation for tape and reel packaging**
- **Lead Free, RoHS Compliant (Optional)**
- **Package Type**
  F = SSOP
- **Revision Designator** (will not correlate with datasheet revision)
- **Device Type**
- **Prefix**
  ICS = Standard Device

0485G—10/13/05



SYMBOL	In Millimeters COMMON DIMENSIONS		In Inches COMMON DIMENSIONS	
	MIN	MAX	MIN	MAX
A	--	1.20	--	.047
A1	0.05	0.15	.002	.006
A2	0.80	1.05	.032	.041
b	0.17	0.27	.007	.011
c	0.09	0.20	.0035	.008
D	SEE VARIATIONS		SEE VARIATIONS	
E	8.10 BASIC		0.319 BASIC	
E1	6.00	6.20	.236	.244
e	0.50 BASIC		0.020 BASIC	
L	0.45	0.75	.018	.030
N	SEE VARIATIONS		SEE VARIATIONS	
α	0°	8°	0°	8°
aaa	--	0.10	--	.004

VARIATIONS

N	D mm.		D (inch)	
	MIN	MAX	MIN	MAX
56	13.90	14.10	.547	.555

Reference Doc.: JEDEC Publication 95, MO-153

10-0039

6.10 mm. Body, 0.50 mm. pitch TSSOP
(240 mil) (20 mil)

Ordering Information

ICS951104yGLFT

Example:

ICS XXXXXX y G LF - T

- **Designation for tape and reel packaging**
- **Lead Free, RoHS Compliant (Optional)**
- **Package Type**
  G = TSSOP
- **Revision Designator** (will not correlate with datasheet revision)
- **Device Type**
- **Prefix**
  ICS = Standard Device

0485G—10/13/05

Revision History

Rev.	Issue Date	Description	Page #
G	10/13/2005	Added LF to Ordering Information	18-19