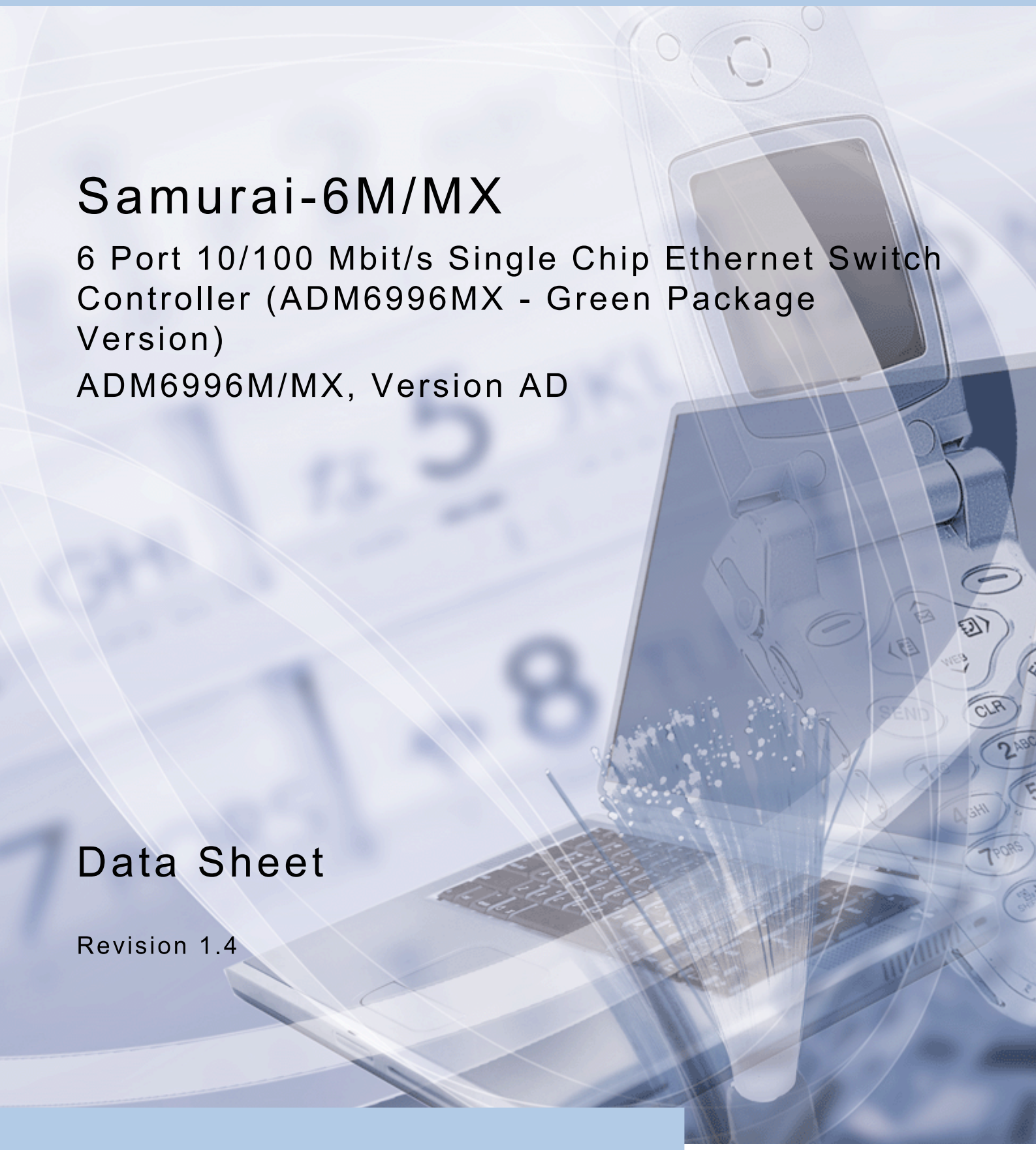
March 2006

Samurai-6M/MX

6 Port 10/100 Mbit/s Single Chip Ethernet Switch Controller (ADM6996MX - Green Package Version)

ADM6996M/MX, Version AD



Data Sheet

Revision 1.4

Communication Solutions

Never stop thinking

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ADM6996M/MX, 6 Port 10/100 Mbit/s Single Chip Ethernet Switch Controller (ADM6996MX - Green Package Version)

Revision History: 2006-03-24, Revision 1.4

Previous Version: Rev. 1.23	
Page/Date	**Subjects (major changes since last revision)**
Page 15	**Rev. 1.2: Modify analog pins number (RXP4-0, RXN4-0, TXP4-0 and TXN4-0)**
Page 81-82	Rev. 1.21: Rearrange $0E_H$ and $0F_H$ registers map
Page 22	Rev. 1.22: Modify LNKFP5 pin description/1_B, Link Failed
2005-07-04	Changed to the new Infineon format
2005-07-04	Rev. 1.22 changed to Rev. 1.23
2005-08-23	Rev 1.3: Update in content
2005-11-01	Revision 1.3 changed to Revision 1.31 Minor change. Included Green package information
2006-03-04	Revision 1.31 changed to Revision 1.4 Modify 3.1.10 Bandwidth Control and add Table 4 Bandwidth Control Timer Select Modify 3.1.15.3 and Figure 5 Configure Samurai QoS Function Correct Figure 10 Full duplex MAC to MAC MII Connection Add 29_H[10:9] register for BCTS and 29_H[8] register for BPM Add thermal resistance information

Trademarks

Table of Contents

List of Figures

List of Tables

1 Product Overview

1.1 Samurai-6M/6MX (ADM6996M/MX) Overview

The Samurai-6M/6MX (ADM6996M/MX) is a high performance, low cost, highly integrated (Controller, PHY and Memory) four 10M/100M auto-detect Half/Full duplex switch ports with TX/FX interfaces and two MII port with one MII supporting GPSI/RMII. The Samurai-6M/6MX (ADM6996M/MX) is intended for applications such as stand alone bridges for the low cost SOHO markets such as 5-port switches and router applications. The Samurai-6MX (ADM6996MX) is the environmentally friendly “green” package version.

The Samurai-6M/6MX (ADM6996M/MX) provides functions such as: 802.1p(Q.O.S.), 802.1Q(VLAN), Port MAC address locking, management, port status, TP auto-MDIX, 25M crystal & extra MII port functions to meet customer requests on switch demand.

The Samurai-6M/6MX (ADM6996M/MX) also supports back pressure in Half-Duplex mode and the 802.3x Flow Control Pause packet in Full-Duplex mode to prevent packet loss when buffers are full. When Back Pressure is enabled, and there is no receive buffer available for the incoming packet, the Samurai-6M/6MX (ADM6996M/MX) will issue a JAM pattern on the receiving port in Half Duplex mode and issue the 802.3x Pause packet back to the receiving end in Full Duplex mode.

The built-in SRAM used for the packet buffer is divided into 256 bytes per block to achieve the optimized memory utilization through complicated link lists on packets with various lengths.

The Samurai-6M/6MX (ADM6996M/MX) also supports priority features using Port-Based, VLAN and IP TOS field checking. Users can easily set different priority modes in individual ports, through a small low-cost micro controller when initializing or configuring on-the-fly. Each output port supports four queues in the way of fixed N: 1 fairness queuing to fit the bandwidth demand on various types of packets such as Voice, Video and Data. 802.1Q, Tag/Untag, and up to 16 groups of VLAN are also supported.

An intelligent address recognition algorithm allows Samurai-6M/6MX (ADM6996M/MX) to recognize up to 2K different MAC addresses and enables filtering and forwarding at full wire speed.

Port MAC address Locking function is also supported by Samurai-6M/6MX (ADM6996M/MX) to use on building Internet access to prevent multiple users sharing one port.

1.2 Features

- Supports four 10M/100M auto-detect Half/Full duplex switch ports with TX/FX interfaces and two MII port with one MII supporting GPSI/RMII
- Supports four 10M/100M auto-detect Half/Full duplex switch ports with TX/FX interfaces, one MII port (for CPU LAN MII) and one isolated PHY(for CPU WAN MII).Five 10M/100M auto-detect Half/Full duplex switch ports with **TX/FX** interfaces
- 2K MAC address tables with 4-ways associative hash algorithm
- 6KX64 bits packet buffers are divided into 192 blocks of 256 bytes each
- Four queues for QoS
- Priority features by Port-Based, 802.1p, IP TOS, Diffserv, TCP/UDP Port Application-Based of packets
- Store & Forward architecture and performs forwarding and filtering at non-blocking full wire speed
- Single/Dual color LED mode with Power On auto diagnostic. Collision/Duplex LED can be separated using register setting
- 802.3x Flow Control pause packet for Full Duplex
- Back Pressure function for Half Duplex operation
- Supports packet lengths up to 1518/1522 (Default)/1536/1784 bytes in maximum
- Scalable Per Port Bandwidth Control (Both Ingress and Egress).
- Broadcast/Multicast Storm Suppression

- 802.1Q VLAN. Up to 16 VLAN groups are implemented by full 12 bits VID matching
- MAC clone function to enable multiple WAN application
- TP interface Auto MDIX function for auto TX/RX swap by strapping-pin.
- Interrupt pin, Interrupt Register and Interrupt Mask Register. Programmable interrupt polarity (Default active low)
- Easy Management 32-bit smart counter for per port RX/TX byte/packet count, 16-bit smart counter for per port ERROR count and Collision count
- Supports 32 hardware IGMP Table (Multicast Table)
- MAC Address Table is accessible
- Supports 802.1x security function
- Supports Spanning Tree Protocol
- Supports internal counter/PHY status output for management system
- 25M Crystal
- 128 QFP package with 0.18 µm technology. 1.8 V/3.3 V power supply.
- 1.0 W low power consumption.

1.3 Applications

Samurai-6M/6MX (ADM6996M/MX):

- SOHO 5-port switch
- 5-port switch + Router with 2 MII CPU interface

1.4 Block Diagram

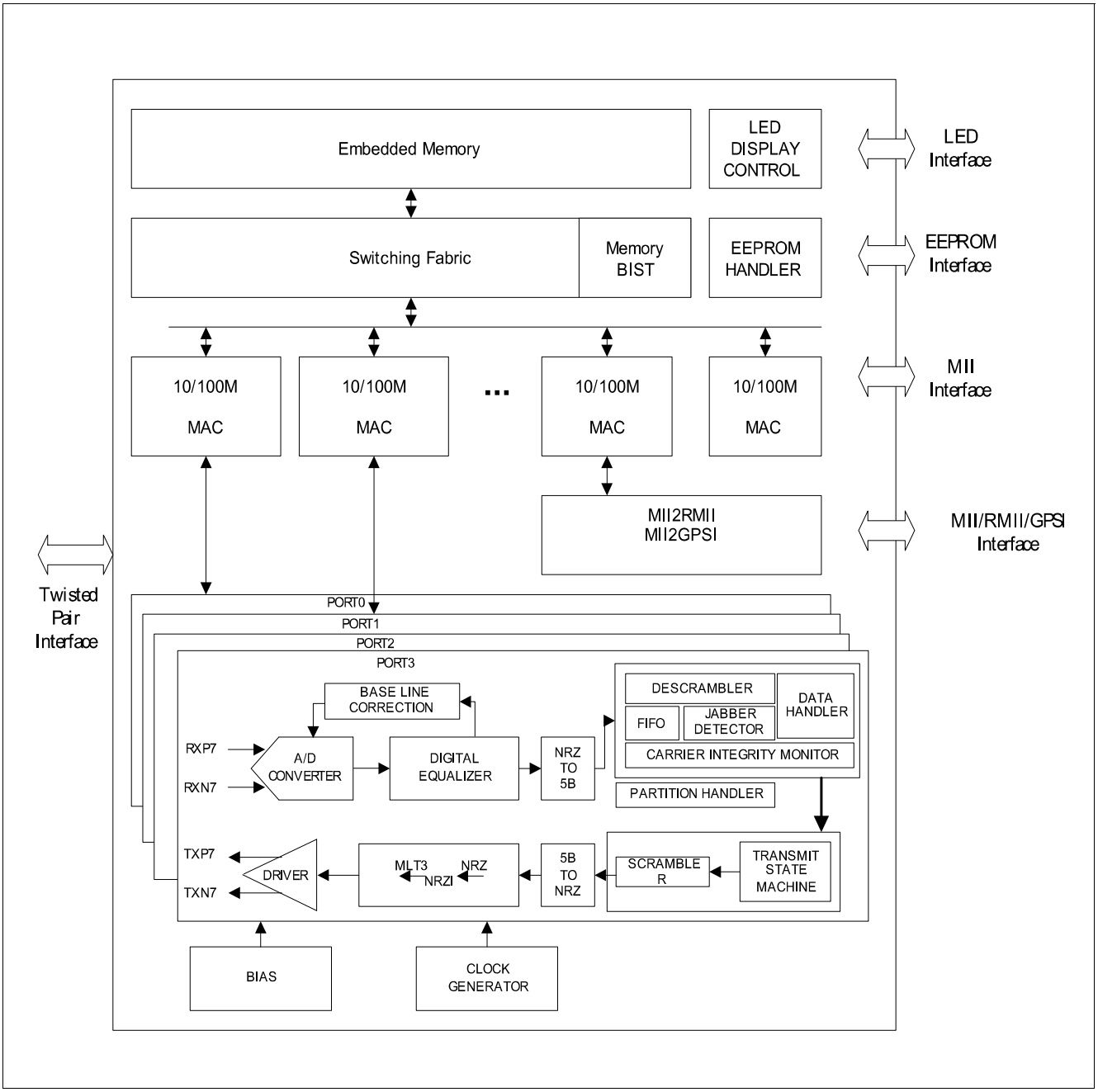

Figure 1 Samurai-6M/6MX (ADM6996M/MX) Block Diagram

1.5 Data Lengths

qword: 64 bits

dword: 32 bits

word: 16 bits

byte: 8 bits

nibble: 4 bits

2 Interface Description

This chapter describes the interface descriptions for the Samurai-6M/6MX (ADM6996M/MX)

- Pin Diagram
- Abbreviations
- Pin Description by Function

2.1 Pin Diagram

Figure 2 shows the pin diagram for the Samurai-6M/6MX (ADM6996M/MX).

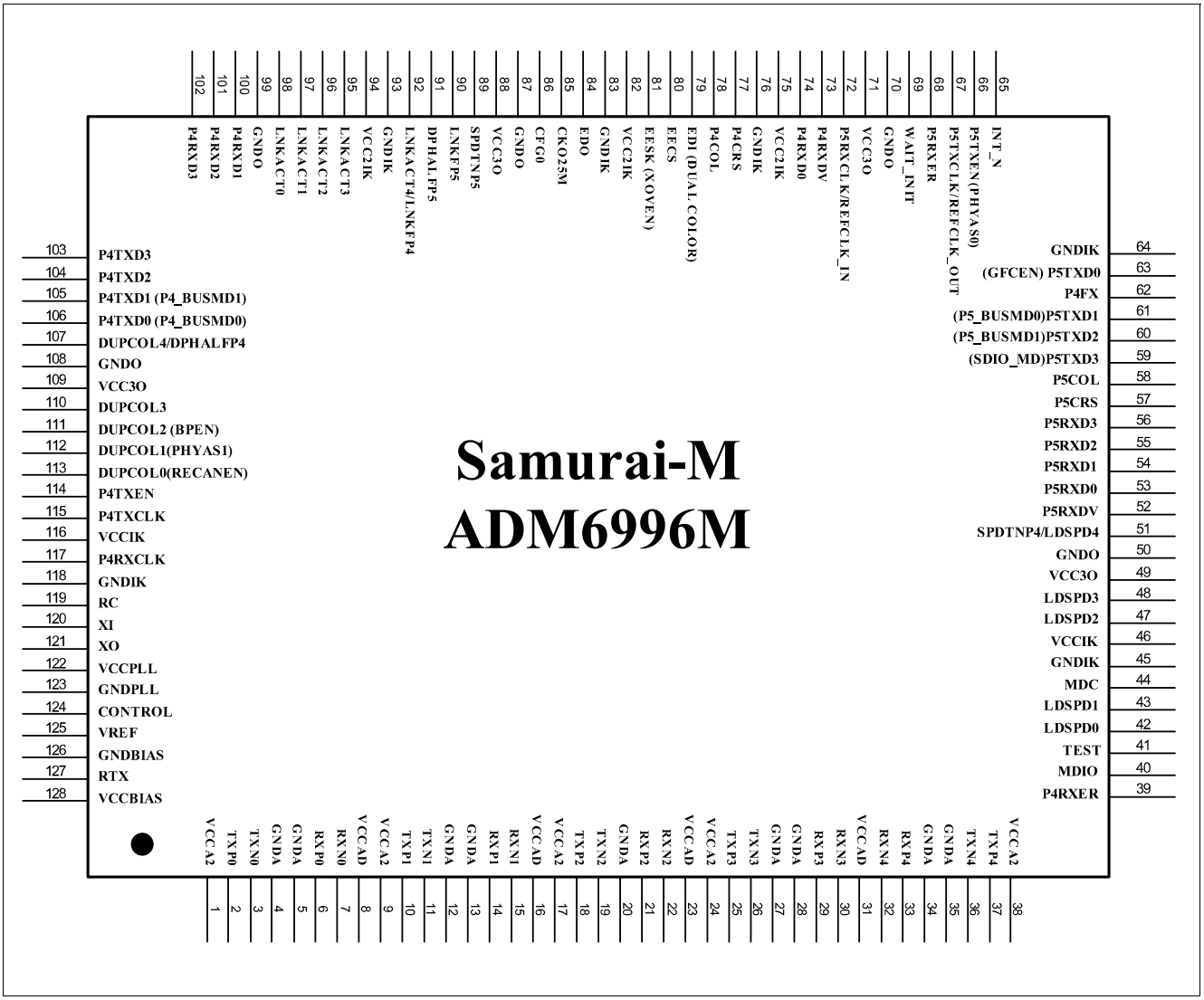

Figure 2 4 TP/FX PORT + 2 MII PORT 128 Pin Diagram

2.2 Abbreviations

Standard abbreviations for I/O tables:

Table 1 Abbreviations for Pin Type

Abbreviations	Description
I	Standard input-only pin. Digital levels.
O	Output. Digital levels.
I/O	I/O is a bidirectional input/output signal.
AI	Input. Analog levels.
AO	Output. Analog levels.
AI/O	Input or Output. Analog levels.
PWR	Power
GND	Ground
MCL	Must be connected to Low (JEDEC Standard)
MCH	Must be connected to High (JEDEC Standard)
NU	Not Usable (JEDEC Standard)
NC	Not Connected (JEDEC Standard)

Table 2 Abbreviations for Buffer Type

Abbreviations	Description
Z	High impedance
PU	Pull up, 10 kΩ
PD	Pull down, 10 kΩ
TS	Tristate capability: The corresponding pin has 3 operational states: Low, high and high-impedance.
OD	Open Drain. The corresponding pin has 2 operational states, active low and tristate, and allows multiple devices to share as a wire-OR. An external pull-up is required to sustain the inactive state until another agent drives it, and must be provided by the central resource.
OC	Open Collector
PP	Push-Pull. The corresponding pin has 2 operational states: Active-low and active-high (identical to output with no type attribute).
OD/PP	Open-Drain or Push-Pull. The corresponding pin can be configured either as an output with the OD attribute or as an output with the PP attribute.
ST	Schmitt-Trigger characteristics
TTL	TTL characteristics

2.3 Pin Description by Function

Samurai-6M/6MX (ADM6996M/MX) pins are categorized into one of the following groups:

- Network Media Connection
- Port 4 MII Interface
- Port 5 MII Interface
- LED Interface
- EEPROM Interface
- Power/Ground, 48 pins
- Miscellaneous