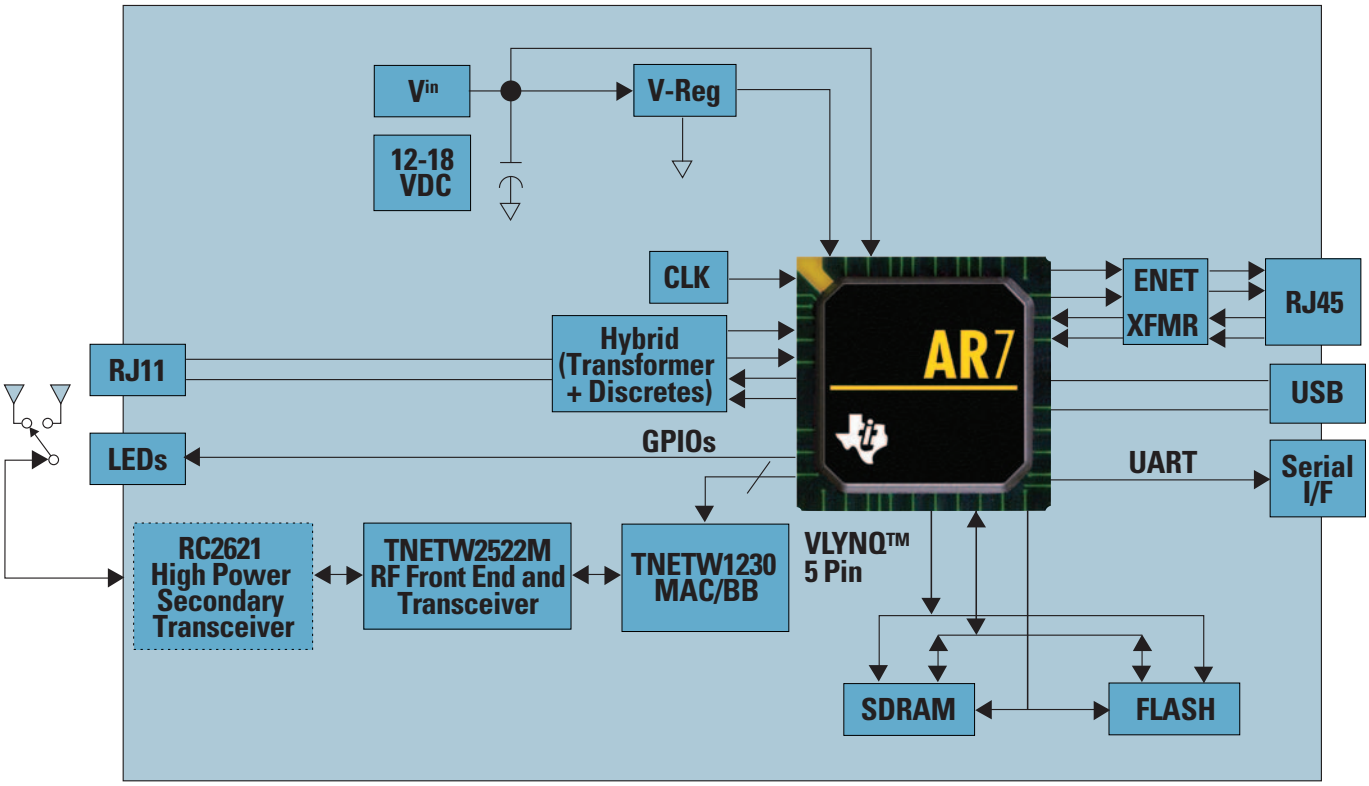
Fact Sheet

AR7Wi Wireless ADSL Router

The AR7Wi chipset is a highly-integrated solution which places all of the needed wireless local area network (WLAN) components on the residential gateway's (RG) motherboard in less than 2.1 square inches of board space. This level of silicon integration enables bill of materials (BOM) cost efficiencies to be passed through to manufacturers, making for an exceedingly cost-competitive RG in the marketplace. In addition, the relatively low number of components in the AR7Wi simplifies assembly and manufacture, while increasing the design's reliability.



AR7

The AR7 device (TNETD7300) is an Asymmetric Digital Subscriber Line (ADSL) bridge/router solution, integrating a broadband communications processor and peripherals, ADSL physical layer, ADSL line driver, USB physical layer, Ethernet physical layer and power management for use in CPE modems for residential and small-office applications. The TNETD7300 can be used in modems ranging from simple Ethernet bridges to integrated access devices (IADs) and RGs. The TNETD7300 includes features to enhance ADSL throughput whenconnected to a compatible central office ADSL modem. ADSL+ provides downstream transmission rates far beyond the 12-Mb/s limit of S=1/2. Extended-Reach (ERADSL) and All Digital Loop ADSL allow 384-kb/s/128-kb/s service to be provided on loops as long as 21 kft. These features allow the TNETD7300 to greatly surpass the downstream throughput limit of 8 Mb/s and the 17.5-kft reach limits generally seen in previous ADSL modems, thus granting ADSL service providers access to a larger subscriber pool without requiring replacement of the local loop infrastructure. The TNETD7300 includes a new VLYNQ™ peripheral bus extension that allows VLYNQ-enabled devices to be gluelessly interfaced to TNETD7300 for advanced applications such as voice-over-packet (VOP) telephony or ADSL-to-WLAN (802.11) bridging and interfaces such as USB 2.0 and PCI.

AR7

MIPS™ 32-Bit 160-MHz Reduced Instruction Set Computer (RISC) Processor

Two IEEE Std. 802.3 Ethernet Memory Access Controllers (MACs) With One External Media Independent Interface (MII)

– IEEE Std. 802.1p/q support
– 10-Mbit/s and 100-Mbit/s (half- or full-duplex)
– Hardware flow control
– Address filtering (Unicast, Multicast, Broadcast, or Promiscuous Mode)

One Integrated IEEE Std. 802.3/802.3u Ethernet PHY

– 10-Mbit/s and 100-Mbit/s (half- or full-duplex)
– Autonegotiation and parallel detect capability

Two VLYNQ™ High-Speed Point-to-Point Serial Interfaces

TMS320C62x™ ADSL PHY Subsystem with Integrated Transceiver, Coder/Decoder (Codec), Line Driver, and Line Receiver

– Single-Core DSP subsystem
– Integrated power management
– Supports most common POTS and ISDN ADSL standards and signaling methods
– ITU 992.1 (G.dmt) Annex A, B, C
– ITU 992.2 (G.lite)
– ITU 992.3 ADSL2 (G.dmt.bis)
– ITU 992.4 ADSL2 (G.lite.bis)
– ANSI T1.413 issue
– Includes ADSL+, Extended-Reach ADSL, All-Digital-Loop ADSL capabilities, Reed-Solomon with S = 1/2

Ethernet MII Serial Management Interface (MDIO)

Flexible Universal Serial Bus (USB) Interface Function

– USB 1.1 compliant slave interface

One Flexible Serial Interface (FSER)

– Configurable as a UART with Software Flow Control or as an Inter-Integrated Circuit (IIC) Master Interface

One Four-Channel General-Purpose Direct-Memory Access (DMA) Engine

Reset Controller

Other Peripherals

– JTAG Test Access Port Controller for IEEE Std.1149 Boundary Scan
– Emulation JTAG (EJTAG) for MIPS
– DSP JTAG interface for debug

Device Packaged in 324-Terminal Thermally-Enhanced Plastic Ball Grid Array (GDW)

Asynchronous Transfer Mode (ATM) Segmentation and Reassembly (SAR) Sublayer

– ATM Adaptation Layer 5 (AAL5) and Operations, Administration and Management (OAM)
– ATM Adaptation Layer 0 (AAL0) support in hardware
– ATM Adaptation Layer 1, 3 and 4 (AAL1, AAL3/4) support via software

ATM Quality of Service (QoS)

– Programmable cell scheduling for AAL5 SAR
– Support for Constant Bit Rate (CBR), Real-Time Variable Bit Rate (VBR-rt), Non-Real-Time Variable Bit Rate (VBR-NRT), and Unspecified Bit Rate (UBR+)

ATM Transmission Convergence

– Automated Idle Cell-Based BERT
– Support for HDLC over ADSL

TNETW1230

The TNETW1230 is a single-chip WLAN MAC and spread-spectrum baseband processor that combines high performance and functionality. The TNETW1230 is available in a 195-terminal GVH/ZVH package with a 12-mm x 12-mm x 1.4-mm form factor. The TNETW1230 supports IEEE Std 802.11a (5-GHz band), 802.11b (2.4-GHz band), and 802.11g (2.4-GHz band) systems, as well as dual-band IEEE Std 802.11a/b and 802.11a/g systems. While the proprietary application of PBCC™ technology in the IEEE Std 802.11b mode of operation provides data rates up to 22 Mbit/s, data rates up to 54 Mbit/s may be provided in IEEE Std 802.11a and 802.11g modes of operation. With its small form factor and low-power features, the TNETW1230 is ideal for WLAN embedded applications.

TNETW2522M

The TNETW2522M is a highly-integrated dual-mode radio designed for 802.11b/g applications incorporating all system blocks from the baseband to the antenna interface except for RF filters. This includes: Power Amplifier (PA), RF detector, T/R switch, Low Noise Amplifier (LNA), Voltage Control Oscillator (VCO) Phase Lock Loop (PLL), PLL reference oscillator, and full RX and TX paths for the 2.4-GHz unlicensed band. Additional features are internal IQ gain and phase balance and DC offset calibration functions and baseband clock generator. The TNETW2522M generates a 40-MHz extremely low jitter clock reference (for baseband A/D converter) using a single 40-MHz crystal.

TNETW2522M

Key Features

- Highly-integrated 802.11b/g radio
- Fully-integrated VCOs and synthesizers, up/down converters, LNA, PA, and T/R switches
- Internal PLL reference oscillator requires only single crystal (no crystal oscillator)
- Integrated transmit temperature compensated coupler-detector
- Generates a 40-MHz clock reference for baseband modem
- Internal AGC, power control and PA bias control functions
- IQ DC offset calibration function and baseband filters integrated
- Excellent jammer immunity
- 6-mm x 10-mm SMT package

Key Specifications

- Receiver sensitivity: -88 dBm
- Output P1dB = +23.5 dBm
- Phase noise 0.5 deg. rms typ. over channel BW
- Single reference frequency: 40 MHz
- Single 3.3 V power supply

TNETW1230

Host Interface

- Provides 16-Bit generic slave-mode operation on host interface
- Supports PCMCIA/CF+ applications
- Supports TI DSL networking and OMAP™ processors through VLYNQ™ interface

Medium-Access Controller (MAC)

- 40- or 80-MHz embedded Advanced RISC Microprocessor (ARM) 7TDMI Central Processing Unit (CPU)
- 120K-Byte embedded Random-Access Memory (RAM)
- Hardware-Based MAC Access Protocol Management
- Hardware-Generated Acknowledgment (ACK), Request to Send (RTS), Clear to Send (CTS), Probe Response, and Beacons
- Hardware-Based Encryption/Decryption using 64-, 128-, and 256-Bit Wired Equivalent Privacy (WEP) keys
- Supports underlying requirements for Wireless Fidelity (Wi-Fi) Protected Access™ (WPA) and IEEE 802.11i draft standard compatibility [Includes Hardware-Accelerated Advanced-Encryption Standard (AES)]
- Supports underlying requirements for IEEE 802.11e draft standard compatibility
- Designed to work with IEEE Std 802.1x for most Virtual Private Network (VPN) solutions

Baseband Processor

- IEEE Std 802.11b data rates: 11 Mbit/s, 5.5 Mbit/s, 2 Mbit/s, 1 Mbit/s [and 22-Mbit/s Packet Binary Convolution Coding (PBCC™)]
- IEEE Std 802.11a and 802.11g Data Rates: 6 Mbit/s, 9 Mbit/s, 12 Mbit/s, 18 Mbit/s, 24 Mbit/s, 36 Mbit/s, 48 Mbit/s, and 54 Mbit/s
- Supports IEEE Std 802.11a, 802.11b, and 802.11g modulations
- Supports IEEE Std 802.11b Short Physical-Layer Convergence Protocol (PLCP) Preambles
- Multipath delay spread tolerance >500 ns RMS

Radio Interface

- Supports Multiple Radio Topologies: IEEE Std 802.11a, 802.11b/g, and dual band
- Analog and digital RX Automatic Gain Control (AGC) outputs
- Analog TX power control
- Implements antenna diversity
- Balanced 20-MHz radio reference clock output

System Level

- Two-wire serial Electrically Erasable Programmable Read-Only Memory (EEPROM) interface
- Supports Auto-Band Multimode WLAN Chipset, allowing operation between 2.4-GHz and 5-GHz frequency bands

RC2621 (optional)

The RC2621 is a fully-integrated high-power 1 Watt Radio Frequency Transmit Receive module (RFTR) designed specifically for use in 802.11b/g applications. The RC2621 is designed to interface with the TNETW2522M to increase radio output power and enhance system receive performance without adding external T/R switches.

The RC2621 incorporates all of the RF blocks for increasing the range of the 802.11b/g radio without adding any external switches or active circuits. The device includes the LNA, PA, bias circuitry, RX gain control, transmit coupler detector, and T/R switches. High integration and internal RF matching enhances performance and greatly reduce external part count. The only external components needed (other than simple passives) for operation are an RF filter and an external low-power DC switching FET.

For More Information

To learn more about the AR7Wi residential gateway solution and TI's other ADSL and 802.11 WLAN products, contact your local TI field sales office or visit www.ti.com/ar7vwi

RC2621

Key Features

- Highly-integrated 802.11b/g Radio Frequency Transmit Receive module
- Fully-integrated LNA, PA, TX coupler detector and T/R switches
- PA Bias Control
- Receive digital gain step
- Integrated temperature compensated TX coupled power detector
- 5-mm x 5-mm LPCC 32 SMT package

Key Specifications

- Antenna port OP1dB = +30 dBm typical
- Antenna port OIP3 = +45 dBm typical
- Frequency range: 2.4 to 2.5 GHz
- Noise figure: 3.5 dB
- Gain: 20 dB TX, 14 dB RX