
AT25F series
AT25DN series
Bios Flash Product Family

Adesto Field Application
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AT25DF and AT25DN Series Offerings

PN	Density	Voltage	Interface	SSH (SOIC 150mil)	MAH (2x3 DFN)	XMH (8-TSSOP)
AT25DN512C	512Kbit	2.3V - 3.6V	SPI & Dual Read	●	●	●

AT25F512B

AT25DN512C

- Single 2.7V - 3.6V Supply
- Serial Peripheral Interface (SPI) Compatible
 - Supports SPI Modes 0 and 3
- 70 MHz Maximum Operating Frequency
 - Clock-to-Output (t_v) of 6 ns Maximum
- Flexible, Optimized Erase Architecture for Code + Data Storage Applications
 - Uniform 4-Kbyte Block Erase
 - Uniform 32-Kbyte Block Erase
 - Full Chip Erase
- Hardware Controlled Locking of Protected Sectors via \overline{WP} Pin
- 128-Byte Programmable OTP Security Register
- Flexible Programming
 - Byte/Page Program (1 to 256 Bytes)
- Fast Program and Erase Times
 - 2.5 ms Typical Page Program (256 Bytes) Time
 - 100 ms Typical 4-Kbyte Block Erase Time
 - 500 ms Typical 32-Kbyte Block Erase Time
- Automatic Checking and Reporting of Erase/Program Failures
- JEDEC Standard Manufacturer and Device ID Read Methodology
- Low Power Dissipation
 - 6 mA Active Read Current (Typical at 20 MHz)
 - 5 μ A Deep Power-Down Current (Typical)
- Endurance: 100,000 Program/Erase Cycles
- Data Retention: 20 Years
- Complies with Full Industrial Temperature Range
- Industry Standard Green (Pb/Halide-free/RoHS Compliant) Package Options
 - 8-lead SOIC (150-mil Wide)
 - 8-pad Ultra Thin DFN (2 x 3 x 0.6 mm)

- Single 2.3V - 3.6V Supply
- Serial Peripheral Interface (SPI) Compatible
 - Supports SPI Modes 0 and 3
 - Supports Dual Output Read
- 85MHz Maximum Operating Frequency
 - Clock-to-Output (t_v) of 7 ns
- Flexible, Optimized Erase Architecture for Code + Data Storage Applications
 - Uniform 256-Byte Page erase
 - Uniform 4-Kbyte Block Erase
 - Uniform 32-Kbyte Block Erase
 - Full Chip Erase
- Hardware Controlled Locking of Protected Sectors via \overline{WP} Pin
- 128-Byte Programmable OTP Security Register
- Flexible Programming
 - Byte/Page Program (1 to 256 Bytes)
- Fast Program and Erase Times
 - 1.5ms Typical Page Program (256 Bytes) Time
 - 50ms Typical 4-Kbyte Block Erase Time
 - 400ms Typical 32-Kbyte Block Erase Time
- Automatic Checking and Reporting of Erase/Program Failures
- Software Controlled Reset
- JEDEC Standard Manufacturer and Device ID Read Methodology
- Low Power Dissipation
 - 200nA Ultra Deep Power Down current (Typical)
 - 5 μ A Deep Power-Down Current (Typical)
 - 25uA Standby current (Typical)
 - 5mA Active Read Current (Typical)
- Endurance: 100,000 Program/Erase Cycles
- Data Retention: 20 Years
- Complies with Full Industrial Temperature Range
- Industry Standard Green (Pb/Halide-free/RoHS Compliant) Package Options
 - 8-lead SOIC (150-mil)
 - 8-pad Ultra Thin DFN (2 x 3 x 0.6 mm)
 - 8-lead TSSOP Package

New

New

Improved

New

New

New

AT25DN512C is backward compatible with AT25F512B command set

Command	AT25F512B opcode	AT25DN512C opcode
Vcc	2.7V - 3.6V	2.3V - 3.6V
Read Array	0Bh	0Bh
Read Array	03h	03h
Dual-Output Read Array		3Bh
Page Erase		81h
Block Erase, 4KB	20h	20h
Block Erase, 32KB	52h	52h
Block Erase, 64KB	D8h	D8h
Chip Erase	60h	60h
Chip Erase	C7h	C7h
Chip Erase (Legacy)	62h	62h
Byte/Page Program	02h	02h
Write Enable	06h	06h
Write Disable	04h	04h
Program OTP Security Register	9Bh	9Bh
Read OTP Security Register	77h	77h
Read Status Register	05h	05h
Write Status Register Byte 1	01h	01h
Write Status Register byte 2		31h
Reset		F0h
Read Manufacturer and Device ID	9Fh	9Fh
Read ID (Legacy)	15h	15h
Deep Power-Down	B9h	B9h
Resume from Deep Power-Down	ABh	ABh
Ultra-Deep Power Down		79h

AT25DN512C Improved Performance and More Package Options

Command	AT25F512B opcode	AT25DN512C opcode
Page Program Time	5 msec Max	5 msec Max
Block Erase, 4KB	250 msec Max	100 msec Max
Block Erase, 32KB	1000 msec Max	800 msec Max
Chip Erase	2 sec Max	2 sec Max
Manufacture and Product ID	1F 65 00 00	1F 65 01 00
Status Register	1 byte	1st byte (same) 2nd byte (new)
SSH, SSU	SSH	SSH
MAH (2x3x0.6mm)	MAH	MAH
XMH (TSSOP)		XMH

New Features

- **The 25DN512C new features**

- **Ultra Deep Power Down Mode**

- Software Controlled Deep Power Down Capability <300nA Standby
- Wake up is H/W controlled and reacts to Edge Transition on Chip Select

- **256Byte Page Erase Capability**

- The 25DN512C supports 4K, 32K sector and Full Chip erase capability
- A new 256Byte Page Erase Capability has been added for even greater flexibility

- **Higher Performance**

- The 512C will operate up to an improved 85Mhz
- The 512C supports Standard SPI protocols and has a new Dual Read Capability

- **Software Controlled Reset Capability**

- The 512C can be RESET using a software SPI command

25F512B – 25DN512C differences

The following change may require software change when migrating from
AT25F512B to AT25DN512C

Product ID:

AT25F512B: 1F 65 00 00
AT25DN512C: 1F 65 01 00

Status Register Read:

- The 512B has a single Byte Status Register
- The 512C has a two Byte Status Register

When Reading the Status Register Byte 1 is the same and 100% Compatible.
Continuously clocking the device will result in byte one being repeated on the 512B, but
the 512C will alternate between byte 1 and byte 2 repeatedly

AT25F512B: Status Reg. Read Sequence : Byte1, Byte1, Byte1, Byte1..
AT25DN512C: Status Reg. Read Sequence : Byte1, Byte2, Byte1, Byte2..

If only Ready/Busy bit is read, it is 100% compatible

25F512B to 25DN512C Part Number X-Reference

- **Table 1 Lists the Primary Datasheet P/N Cross References**

EOL Part Number	Replacement Part Number	Carrier Type
AT25F512B-MAH-Y	AT25DN512C-MAHF-Y	Y for Tray
AT25F512B-MAH-T	AT25DN512C-MAHF-T	T for T/R
AT25F512B-SSH-B	AT25DN512C-SSHF-B	B for Bulk
AT25F512B-SSH-T	AT25DN512C-SSHF-T	T for T/R
AT25F512B-XH-B	AT25DN512C-XMHF-B	B for Bulk
AT25F512B-XH-T	AT25DN512C-XMHF-T	T for T/R
AT25BCM512B-MAH-T	AT25DN512C-MAHF-T	T for T/R

Notes:

1. The carrier type is not marked on the package.
2. Table 1 lists standard datasheet part numbers only.

This Table does not list ALL SLxxx codes and possible ordering code options